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Datasheet

AUO

A030VAN03.0

UP-02-206

Company Name

MODEL A030VAN03.0

CUSTOMER APPROVED

■ APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver. 1.0)

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Product Specification

3.0″ COLOR TFT-LCD MODULE

Model Name : A030VAN03.0

Planned Lifetime:

Phase-out Control:

EOL Schedule:

< > Preliminary Specification

< ◆ > Final Specification

Note: The content of this specification is subject to change without prior notice.

Record of Revision

Version	Revise Date	Page	Content
1.0	2018/03/05		EC Nitto polarizer
			Update AUO part number

Contents

Precaution in Design

1. Notice

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2) The application examples in these specification sheets are provided to explain the representative applications of the device and are not intended to guarantee any industrial property right or other rights or license you to use them. AUO assumes no responsibility for any problems related to any industrial property right of a third party resulting from the use of the device.

3) The device listed in these specification sheets was designed and manufactured for use in Telecommunication equipment (terminals)

4) In case of using the device for applications such as control and safety equipment for transportation (aircraft, trains, automobiles, etc.), rescue and security equipment and various safety related equipment which require higher reliability and safety, take into consideration that appropriate measures such as fail-safe functions and redundant system design should be taken.

5) Do not use the device for equipment that requires an extreme level of reliability, such as aerospace applications, telecommunication equipment (trunk lines), nuclear power control equipment and medical or other equipment for life support.

6) AUO assumes no responsibility for any damage resulting from the use of the device which does not comply with the
instructions and the precautions specified in these specification sheets.

7) Contact and consult with a AUO sales representative for any questions about this device.

. Operating Precautions

1) Since front polarizer is easily damaged, please be cautious and not to scratch it.

2) Be sure to turn off power supply when inserting or disconnecting from input connector.

3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

4) When the panel surface is soiled, wipe it with absorbent cotton or soft cloth.

5) Since the panel is made of glass, it may be broken or cracked if dropped or bumped on hard surface.

6) Do not open nor modify the module assembly.

7) Do not press the reflector sheet at the back of the module to any direction.

8) In case if a module has to be put back into the packing container slot after it was taken out from the container, do not press the center of the LED light bar edge. Instead, press at the far ends of the LED light bar edge softly. Otherwise the TFT Module may be damaged.

2. For Handing And System Design

1) Do not scratch the surface of the polarizer film as it is easily damaged.
2) If the cleaning of the surface of the LCD panel is necessary, wipe it swiftly with cotton or other soft cloth. Do not use organic solvent as it damages polarizer.
3) Water droplets on polarizer must be wiped off immediately as they may cause color changes, or other defects if remained for a long time.
4) Since this LCD panel is made of glass, dropping the module or banging it against hard objects may cause cracks or fragmentation.
5) Certain materials such as epoxy resin (amine' s hardener) or silicone adhesive agent (de-alcohol or de-oxym) emits gas to which polarizer reacts (color change). Check carefully that gas from materials used in system housing or packaging do not hart polarizer.
6) Liquid crystal material will freeze below specified storage temperature range and it will not get back to normal quality even after temperature comes back within specified temperature range. Liquid crystal material will become isotropic above specified temperature range and may not get back to normal quality. Keep the LCD module always within specified temperature range.
7) Do not expose LCD module to the direct sunlight or to strong ultraviolet light for long time.
8) If the LCD driver IC (COG) is exposed to light, normal operation may be impeded. It is necessary to design so that the light is shut off when the LCD module is mounted.
9) Do not disassemble the LCD module as it may cause permanent damage.
10) As this LCD module contains components sensitive to electrostatic discharge, be sure to follow the instructions in below.

① Operators

Operators must wear anti-static wears to prevent electrostatic charge up to and discharge from human body.

② Equipment and containers

Process equipment such as conveyer, soldering iron, working bench and containers may possibly generate electrostatic charge up and discharge. Equipment must be grounded through 100Mohms resistance. Use ion blower.

③ GND

To avoid ESD (Electro Static Discharge) damage, be sure to ground yourself before handling TFT- LCD Module.

④Humidity

Proper humidity of working room may reduce the risk of electrostatic charge up and discharge. Humidity should be kept over 50% all the time.

⑤Transportation/storage

Storage materials must be anti-static to prevent causing electrostatic discharge.

⑥Others

Protective film is attached on the surface of LCD panel to prevent scratches or other damages. When removing this protective film, remove it slowly under proper anti-ESD control such as ion blower.

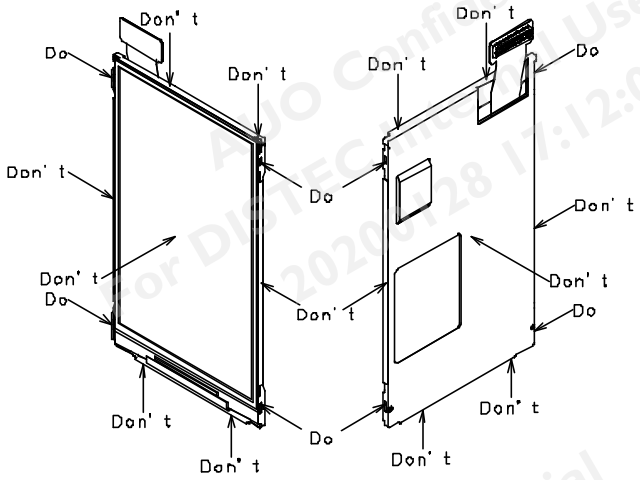
11) Hold LCD very carefully when placing LCD module into the system housing. Do not apply excessive stress

or pressure to LCD module. Do not to use chloroprene rubber as it may affect on the reliability of the electrical interconnection.

12) Do not hold or touch LCD panel to flex interconnection area as it may be damaged.

13) As the binding material between LCD panel and flex connector mentioned in 12) contains an organic material, any type of organic solvents are not allowed to be used. Direct contact by fingers is also prohibited.

14) When carrying the LCD module, place it on the tray to protect from mechanical damage. It is recommended to use the conductive trays to protect the CMOS components from electrostatic discharge. When holding the module, hold the Plastic Frame of LCD module so that the panel, COG and other electric parts are not damaged.



15) Place a protective cover on the LCD module to protect the glass panel from mechanical damages.

16) LCD panel is susceptible to mechanical stress and even the slightest stress will cause a color change in background. So make sure the LCD panel is placed on flat plane without any continuous twisting, bending or pushing stress.

17) Protective film is placed onto the surface of LCD panel when it is shipped from factory. Make sure to peel it off before assembling the LCD module into the system. Be very careful not to damage LCD module by electrostatic discharge when peeling off this protective film. Ion blower and ground strap are recommended.

18) Make sure the mechanical design of the system in which the LCD module will be assembled matches specified viewing angle of this LCD module.

19) This LCD module does not contain nor use any ODS (1,1,1-Trichloroethane, CCL4) in all materials used, in all production processes.

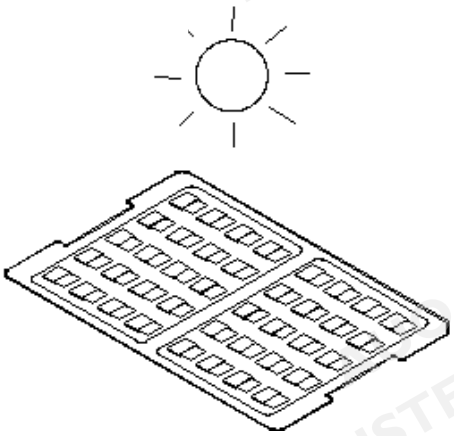
3. For Operating LCD Module

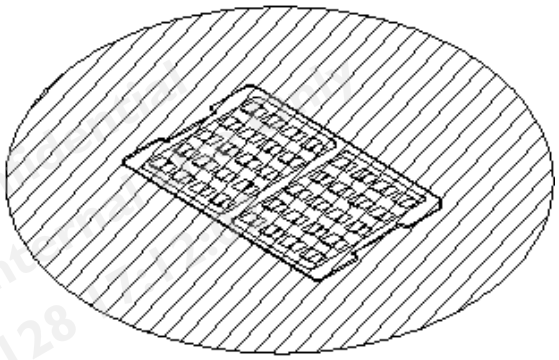
1) Do not operate or store the LCD module under outside of specified environmental conditions.
2) At the shipment, adjust the contrast of each LCD module with electric volume. LCD contrast may vary from panel to panel depending on variation of LCD power voltage from system.
3) As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 ˚C and it becomes stable.

4. Precaution For Storage

1) Do not expose the LCD module to direct sunlight or strong ultraviolet light for long periods. Store in a dark place.
2) The liquid crystal material will solidify if stored below the rated storage temperature and will become an isotropic liquid if stored above the rated storage temperature, and may not retain its original properties. Only store the module at normal temperature and humidity (25±5˚C,60±10%RH) in order to avoid exposing the front polarizer to chronic humidity.
3) Keeping Method

DON'T DO





a. Don't keeping under the direct sunlight. b. Keeping in the tray under the dark place.

4) Do not operate or store the LCD module under outside of specified environmental conditions.
5) Be sure to prevent light striking the chip surface.

5. Other Notice

1) Do not operate or store the LCD module under outside of specified environmental conditions.
2) As electrical impedance of power supply lines (VCC-GND) are low when LCD module is working, place the de-coupling capacitor near by LCD module as close as possible.
3) Reset signal must be sent after power on to initialize LSI. LSI does not function properly until initialize it by reset signal.
4) Generally, at power on, in order not to apply DC charge directly to LCD panel, supply logic voltage first and initialize LSI logic function including polarity alternation. Then supply voltage for LCD bias. At power off, in order not to apply DC charge directly to LCD panel, execute Power OFF sequence and Discharge command.
5) Don’ t touch to FPC surface, exposed IC chip, electric parts and other parts, to any electric, metallic materials.
6) No bromide specific fire-retardant material is used in this module.
7) Do not display still picture on the display over 2 hours as this will damage the liquid crystal.
8) The connector used in this LCD module is the one AUO have not ever used.

Therefore, please note that the quality of this connector concerned is out of AUO's guarantee.

6. Precaution for Discarding Liquid Crystal Modules

COG: After removing the LSI from the liquid crystal panel, dispose of it in a similar way to circuit boards from electronic devices.

LCD panel: Dispose of as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal panel only contains an extremely small amount of liquid crystal (approx.100mg) and therefore it will not leak even if the panel should break.

-Its median lethal dose (LD50) is greater than 2,000 mg/kg and a mutagenetic (Aims test: negative) material is employed.

A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution（dot）	640 (W) x 480 RGB (H)	
2	Active area（mm）	60(W) x 45(H)	
3	Screen size（inch）	2.95 (Diagonal)	
4	Dot pitch（um）	93.75 x 93.75	
5	Color configuration	R, G, B Stripe	
6	Overall dimension（mm）	71.4(W) x 51(H) x 2.2(D)	Note 1
7	Weight（g）	17.6	
8	Panel surface treatment	AR<=1.5%	
9	Frame Rate	50Hz / 60HZ	Note 2

Note 1: Refer to section F Outline Dimension

Note 2: Refer to section B input timing and section G power on/off sequence

B. Electrical specifications

1. Pin assignment

Compatible Connector : Molex 503566-4500

Pin no	Symbol	I/O	Pin type	Description	Remark
1	RESX	I	Type 1	Global reset pin	
2	CS	I	Type 1	Serial communication chip select	
3	SDA	I/O	Type 2	Serial communication data input	
4	SCL	I	Type 1	Serial communication clock input	
5	VSYNC	I	Type 1	Vertical sync signal	
6	HSYNC	I	Type 1	Horizontal sync signal	
7	Test pin1	D	-	Not connected	
8	VDDIO	P	-	Voltage input pin for digital power	
9	GND	P	-	Ground	
10	DR7	I	Type 3	Red Data signal (MSB)	Note1
11	DR6	I	Type 3	Red Data signal	Note1
12	DR5	I	Type 3	Red Data signal	Note1
13	DR4	I	Type 3	Red Data signal	Note1
14	DR3	I	Type 3	Red Data signal	Note1
15	DR2	I	Type 3	Red Data signal	Note1
16	DR1	I	Type 3	Red Data signal	Note1
17	DR0	I	Type 3	Red Data signal (LSB)	Note1
18	GND	P	-	Ground	
19	DG7	I	Type 3	Green Data signal (MSB)	Note2
20	DG6	I	Type 3	Green Data signal	Note2
21	DG5	I	Type 3	Green Data signal	Note2
22	DG4	I	Type 3	Green Data signal	Note2
23	DG3	I	Type 3	Green Data signal	Note2
24	DG2	I	Type 3	Green Data signal	Note2
25	DG1	I	Type 3	Green Data signal	Note2
26	DG0	I	Type 3	Green Data signal (LSB)	Note2
27	GND	P	-	Ground	
28	DB7	I	Type 3	Blue Data signal (MSB)	Note3
29	DB6	I	Type 3	Blue Data signal	Note3
30	DB5	I	Type 3	Blue Data signal	Note3

31	DB4	I	Type 3	Blue Data signal	Note3
32	DB3	I	Type 3	Blue Data signal	Note3
33	DB2	I	Type 3	Blue Data signal	Note3
34	DB1	I	Type 3	Blue Data signal	Note3
35	DB0	I	Type 3	Blue Data signal (LSB)	Note3
36	GND	P	-	Ground	
37	DCLK	I	Type 3	Clock signal	
38	GND	P	-	Ground	
39	Test pin2	D	-	Not connected	
40	Test pin3	D	-	Not connected	
41	VDD	P	-	Voltage input pin for analog power	
42	Test pin4	D	-	Not connected	
43	Test pin5	D	-	Not connected	
44	LED-	P	-	LED backlight cathode	
45	LED+	P	-	LED backlight anode	

I：Input, C：Capacitor, P：Power, D：Dummy

Note1:DR[7:0]: When input timing is ‘Parallel RGB’, it is as Red digital data input.

When input timing is ‘YUV’, it is as C-data input.

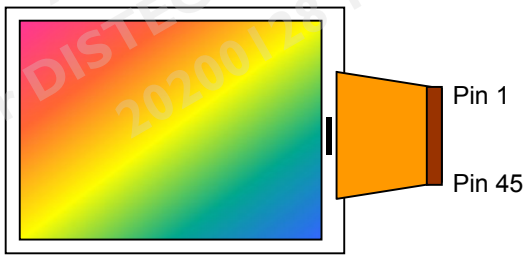
Note2:DG[7:0] : When input timing is ‘Parallel RGB’, it is as Green digital data input.

When input timing is ‘YUV’, it is as Y-data input.

Note3:DB[7:0] :When input timing is ‘Parallel RGB’, it is as Blue digital data input.

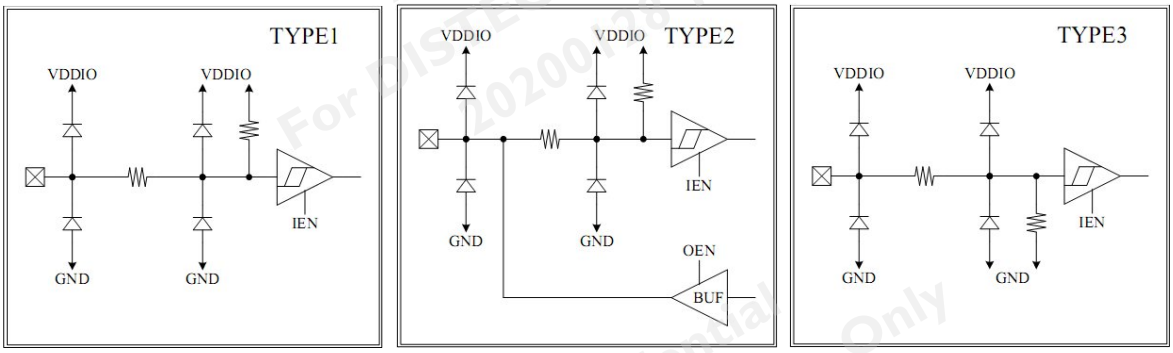
When input timing is ‘YUV’, it is as floating or pull low.

Note4:Definition of scanning direction, Refer to figure as below：



I/O Pin Type:

Pull high/low resistor is **700kΩ.**



2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Supply Voltage	VDD	GND=0V	-0.3	5.0	V	
Supply Voltage	VDDIO	GND=0V	-0.3	5.0	V	

Note : If the operating condition exceeds the absolute maximum ratings, the TFT-LCD module may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, its reliability may drop.

3. Electrical characteristics

3.1 Recommended operating conditions (GND=0V)

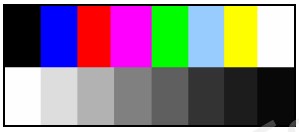
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power Supply		VDD	3.0	3.3	3.6	V	
		VDDIO	1.7	1.8	VDD	V	
Input Signal voltage	H Level	V_{IH}	0.7* VDDIO	-	VDDIO	V	
	L Level	V_{IL}	GND	-	0.3* VDDIO	V	

3.2 Electrical characteristics (GND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input Current for VDD	I_{VDD}	VDD=3.3V	-	17	22	mA	
	$I_{VDD(STANDBY)}$		-	0.1	0.2	mA	
Input Current for VDDIO	I_{VDDIO}	VDDIO=1.8V	-	1	3	mA	
	$I_{VDDIO(STANDBY)}$		-	0.1	0.2	mA	

Note1: Test Condition is under typical Eletrical DC and AC characteristics.

Note2: Test Condition: 8colorbar+Grayscale pattern, Frame rate: 60Hz, other registers are default setting.

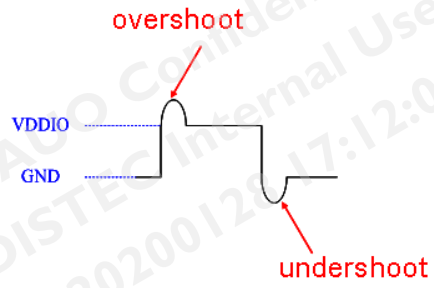


Note 3: In standby mode, all digital signals are stopped. Ex. DCLK, HSYNC ..etc.

3.3 Digital input signal overshoot and undershoot limitation

The digital input signal overshoot and undershoot voltage should keep under VDDIO+0.2V and over GND-0.2V.

Symbol	Overshoot	Undershoot
DB[7:0]	< VDDIO+0.2V	> GND-0.2V
DG[7:0]		
DR[7:0]		
DCLK		
HSYNC/VSYNC		
SCL/ SDA/ CS		



3.4 Recommended Capacitance Values of External Capacitor

The recommended capacitance values of the external capacitor are shown below. These values should be finally determined only after performing sufficient evaluation on the module.

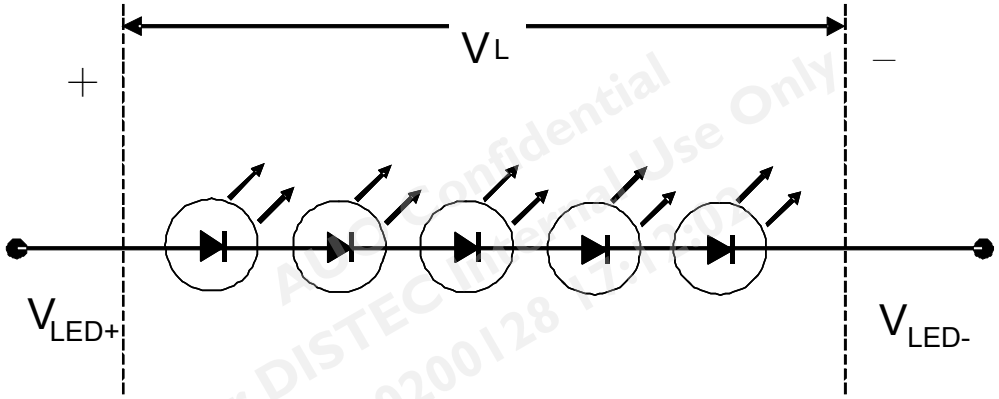
Pin name	Value	Max ability
VDD	Cap , 2.2uF	6.3V
VDDIO	Cap , 2.2uF	6.3V

3.5 Backlight driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current		-	20	22.5	mA	
LED voltage	V_L	-	14.75		V	5 LED's

Note1: To consider LED driver and feedback resistor tolerance.

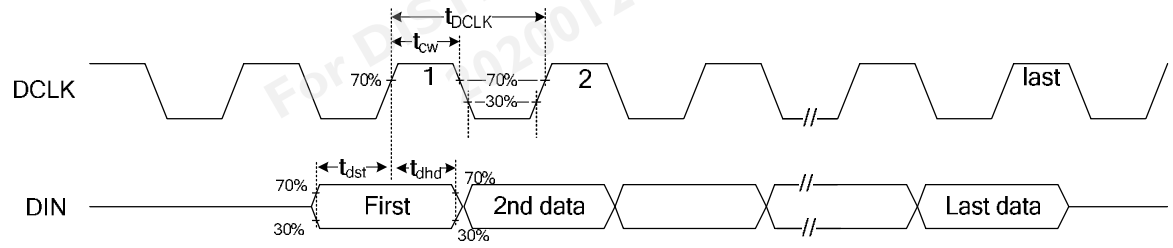
Note2: If using LCD internal LED driver controller the maximum setting should be typical value. Ta=25℃

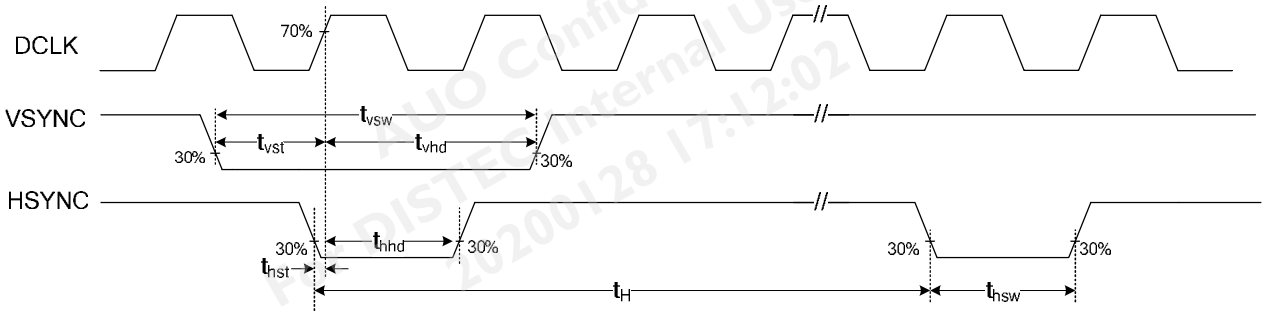


4. Input timing AC characteristic

(VDD=3.0V~3.6V, VDDIO=1.7V~VDD, GND=0V, Top=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK duty cycle	tcw	40	50	60	%	
VSYNC setup time	tvst	10	-	-	ns	
VSYNC hold time	tvhd	10	-	-	ns	
VSYNC width	tvsw	1	-	-	t_H	
HSYNC setup time	thst	10	-	-	ns	
HSYNC hold time	thhd	10	-	-	ns	
HSYNC width	thsw	1	-	-	t_{DCLK}	
Data setup time	tdst	10	-	-	ns	
Data hold time	tdhd	10	-	-	ns	





t_H means: HSYNC period

5. Input timing format

5.1 Parallel RGB timing, frame rate is 60Hz (Refer to Fig.1 and Fig.2)

Parameter		Symbo	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency		$1/t_{DCLK}$	20.00	22.05	23.98	MHz	
HSYNC	Period	t_H	660	700	740	t_{DCLK}	
	Display period	t_{hd}		640		t_{DCLK}	
	Blanking	t_{hb}	10	40	70	t_{DCLK}	Note 1
	Front porch	t_{hfp}	10	20	30	t_{DCLK}	
	Pulse width	t_{hsw}	1	1	t_{hb-1}	t_{DCLK}	
VSYNC	Period	t_V	505	525	540	t_H	
	Display period	t_{vd}		480		t_H	
	Blanking	t_{vb}	7	21	30	t_H	Note 2
	Front porch	t_{vfp}	18	24	30	t_H	
	Pulse width	t_{vsw}	1	1	t_{vb}-1	t_H	
Frame rate		$1/t_v$	60	60	60	Hz	

5.1 Parallel RGB timing, frame rate is 50Hz (Refer to Fig.1 and Fig.2)

Parameter		Symbo	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency		$1/t_{DCLK}$	-	18.38	19.98	MHz	
HSYNC	Period	t_H	-	700	740	t_{DCLK}	
	Display period	t_{hd}		640		t_{DCLK}	
	Blanking	t_{hb}	-	40	70	t_{DCLK}	Note 1
	Front porch	t_{hfp}	-	20	30	t_{DCLK}	
	Pulse width	t_{hsw}	-	1	t_{hb-1}	t_{DCLK}	
VSYNC	Period	t_V	-	525	540	t_H	
	Display period	t_{vd}		480		t_H	
	Blanking	t_{vb}	-	21	30	t_H	Note 2
	Front porch	t_{vfp}	-	24	30	t_H	
	Pulse width	t_{vsw}	-	1	t_{vb}-1	t_H	
Frame rate		$1/t_v$	-	50	50	Hz	

Note 1: The t_{hb} time is adjustable by setting register HBLANKING; requirement of minimum blanking time and minimum front porch time must be satisfied.

Note 2: The t_{vb} time is adjustable by setting register VBLANKING.

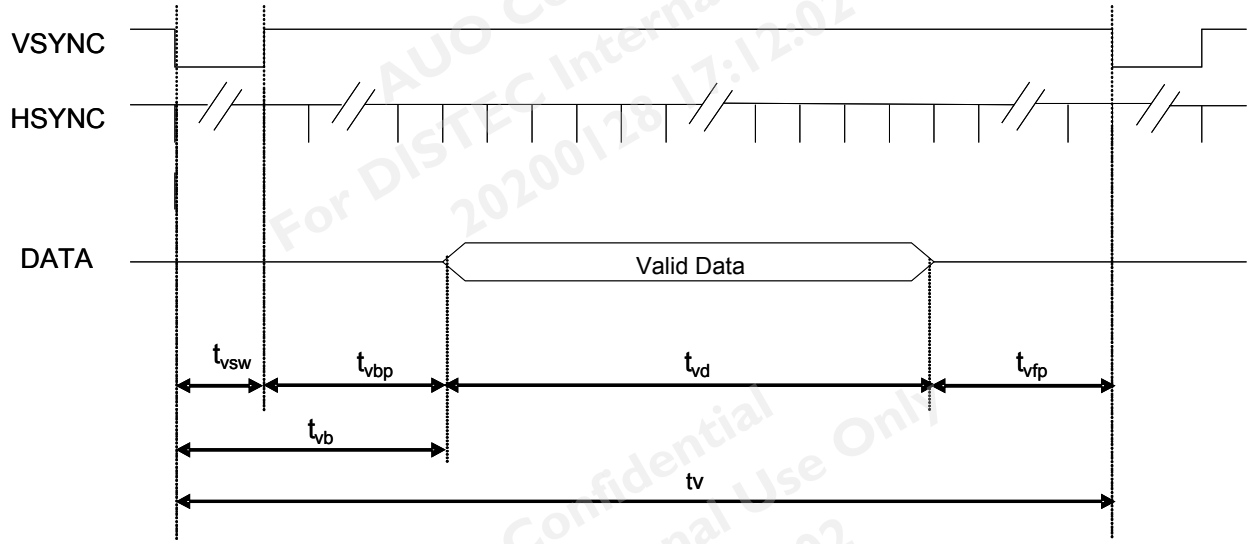


Fig.1 Parallel RGB Input Vertical Timing Chart

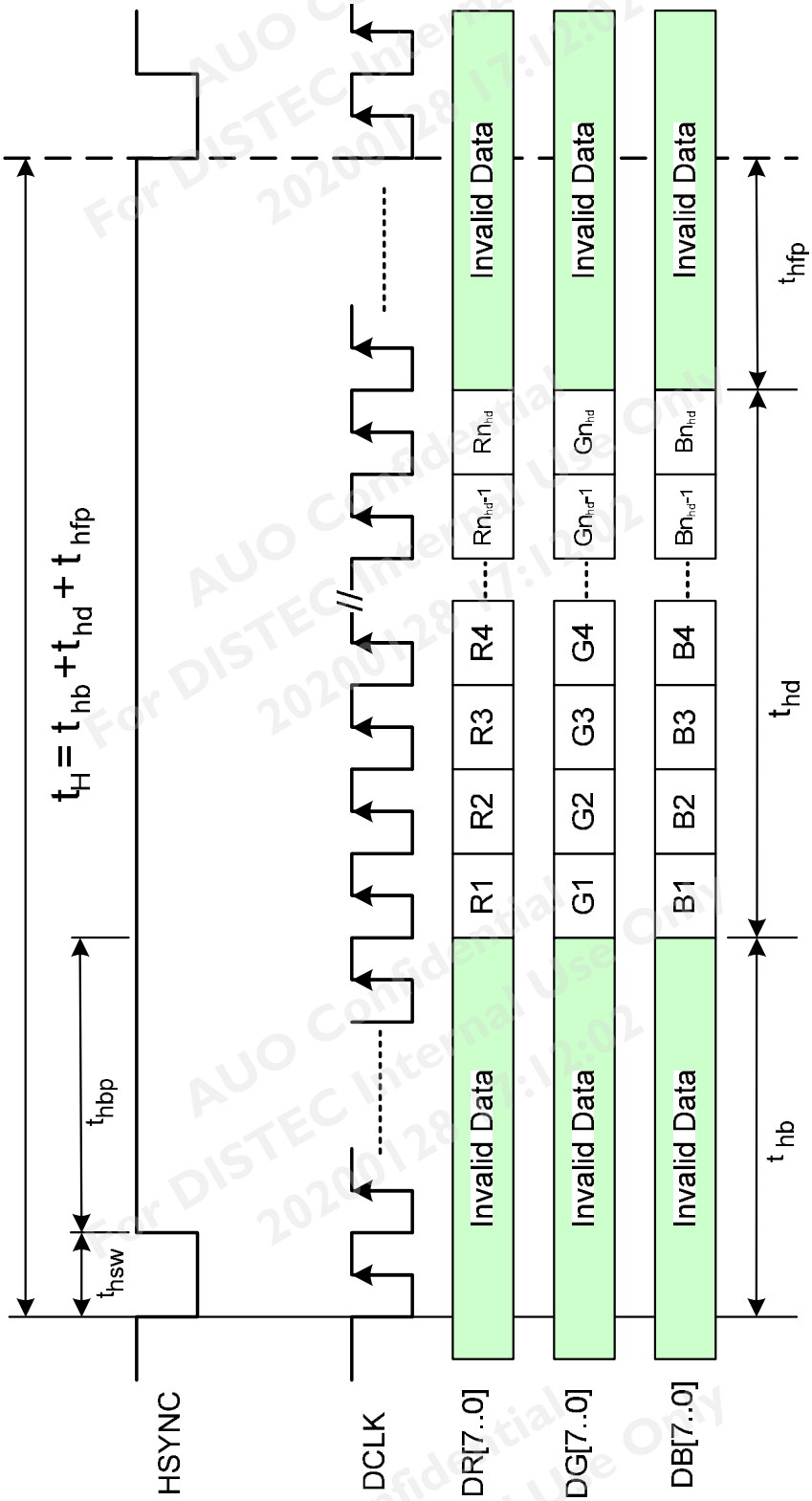


Fig.2 Parallel RGB Input Horizontal Timing Chart

5.2 YUV 16-bit timing, frame rate is 60Hz (Refer to Fig.3 and Fig.4)

Parameter		Symbo	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency		$1/t_{DCLK}$	24.1	27.0	28.4	MHz	
HSYNC	Period	t_H	810	857	880	t_{DCLK}	
	Display period	t_{hd}		640		t_{DCLK}	
	Blanking	t_{hb}	20	40	60	t_{DCLK}	Note 1
	Front porch	t_{hfp}	150	177	180	t_{DCLK}	
	Pulse width	t_{hsw}	1	1	T_{hpb}-1	t_{DCLK}	
VSYNC	Period	t_V	496	525	538	t_H	
	Display period	t_{vd}		480		t_H	
	Blanking	t_{vb}	11	21	26	t_H	Note 2
	Front porch	t_{vfp}	5	24	32	t_H	
	Pulse width	t_{vsw}	1	1	t_{vbp}-1	t_H	
Frame rate		$1/t_v$	60	60	60	Hz	

5.2 YUV 16-bit timing, frame rate is 50Hz (Refer to Fig.3 and Fig.4)

Parameter		Symbo	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency		$1/t_{DCLK}$	-	22.5	23.7	MHz	
HSYNC	Period	t_H	-	857	880	t_{DCLK}	
	Display period	t_{hd}		640		t_{DCLK}	
	Blanking	t_{hb}	-	40	60	t_{DCLK}	Note 1
	Front porch	t_{hfp}	-	177	180	t_{DCLK}	
	Pulse width	t_{hsw}	-	1	T_{hpb}-1	t_{DCLK}	
VSYNC	Period	t_V	-	525	538	t_H	
	Display period	t_{vd}		480		t_H	
	Blanking	t_{vb}	-	21	26	t_H	Note 2
	Front porch	t_{vfp}	-	24	32	t_H	
	Pulse width	t_{vsw}	-	1	t_{vbp}-1	t_H	
Frame rate		$1/t_v$	-	50	50	Hz	

Note 1: The t_{hb} time is adjustable by setting register HBLANKING; requirement of minimum blanking time and minimum front porch time must be satisfied.

Note 2: The t_{vb} time is adjustable by setting register VBLANKING.

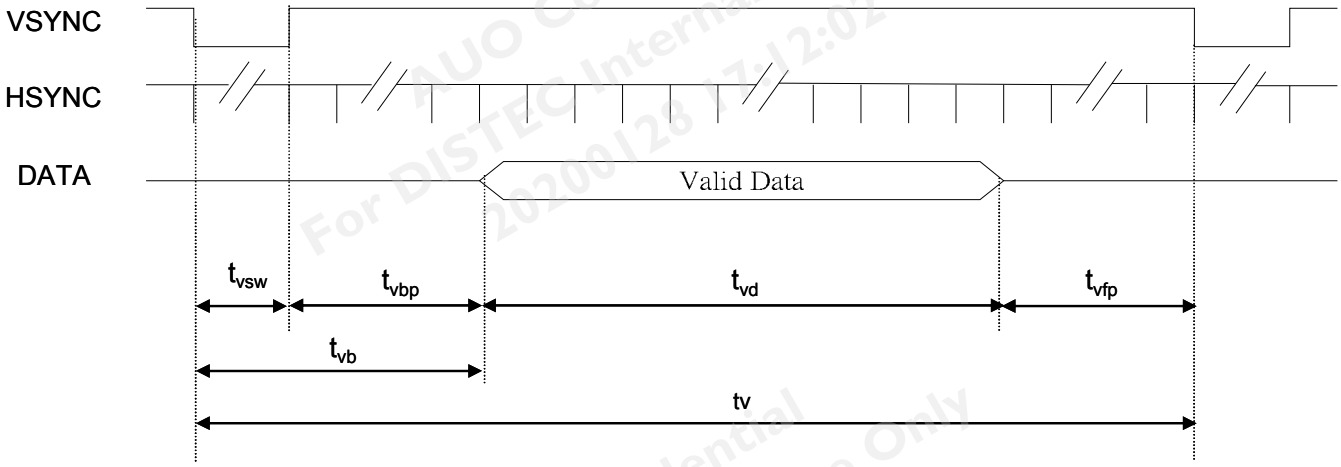


Fig.3 YUV Input Vertical Timing Chart

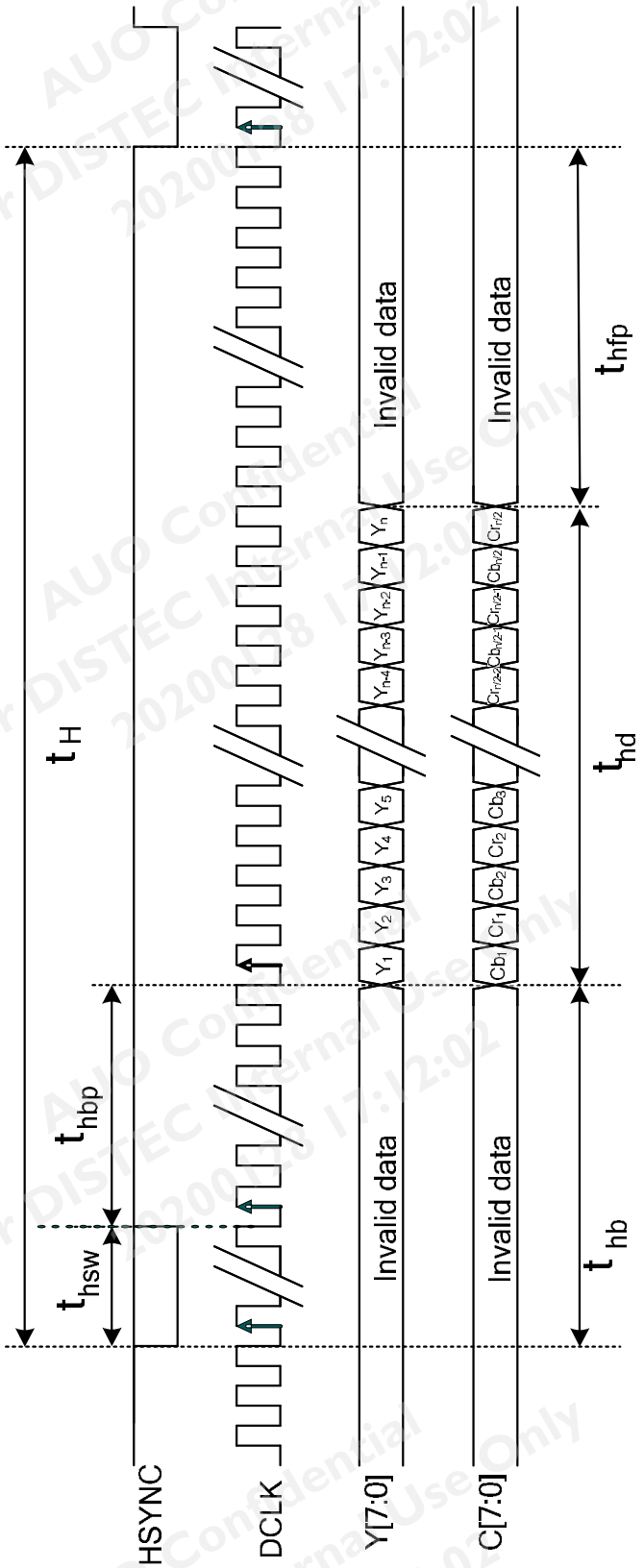
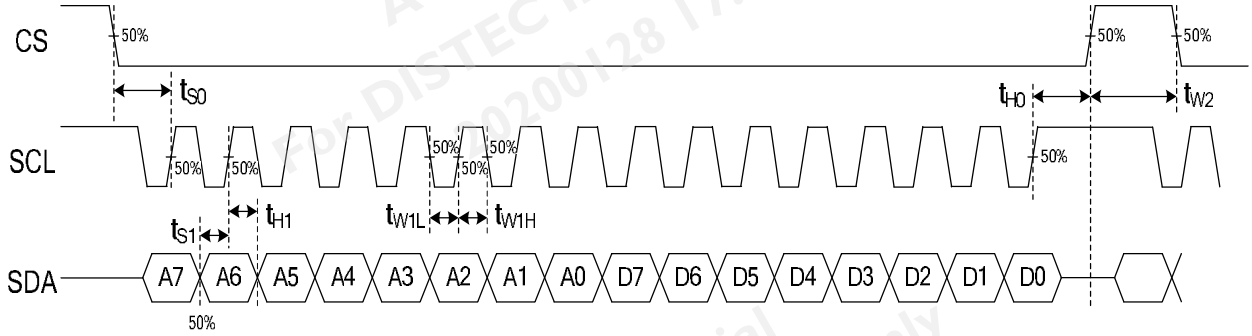


Fig.4 YUV Input Horizontal Timing Chart

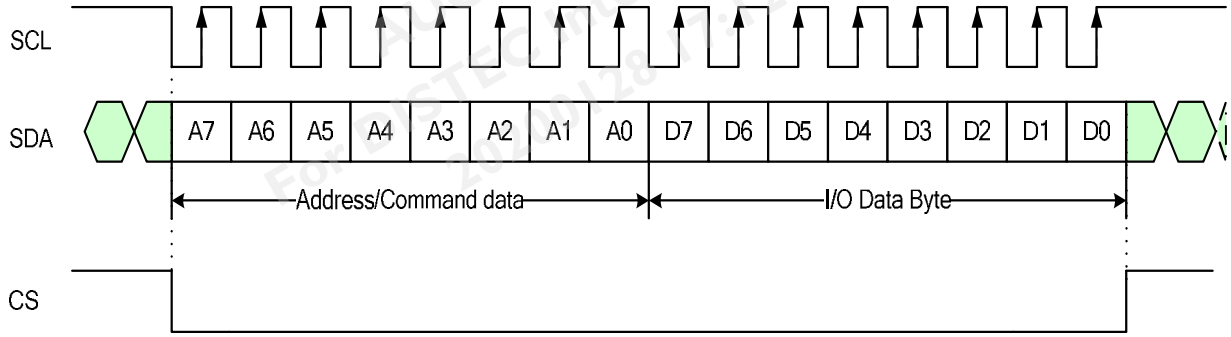
6. Serial peripheral interface

6.1 AC characteristic



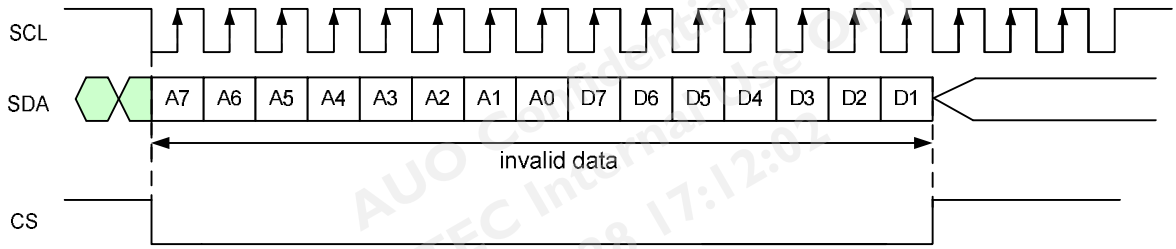
Item	Symbol	Min	Typical	Max	Unit
CS input setup Time	t_{S0}	100	-	-	ns
CS input hold Time	t_{H0}	100	-	-	ns
CS pulse high width	t_{W2}	400	-	-	ns
SCL pulse low width	t_{W1L}	100	-	-	ns
SCL pulse high width	t_{W1H}	100	-	-	ns
SDA input setup Time	t_{S1}	100	-	--	ns
SDA input hold Time	t_{H1}	100	-	-	ns

6.2 Timing chart

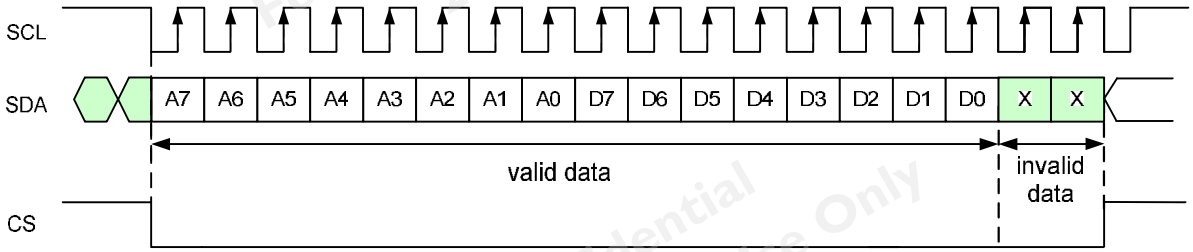


1. Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.
2. Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.
3. If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.(Note1)
4. If 16 bits or more of SCL are input while CS is low, the previous 16 bits of transferred data after the falling edge of CS pulse are valid data.(Note2)
5. Serial block operates with the SCL clock.
6. Serial data can be accepted in the standby (power save) mode.

Note1: data<16bits



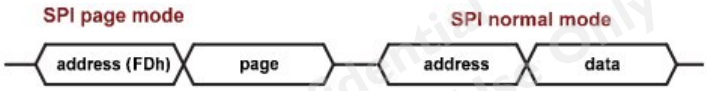
Note2: data>16bits



6.3 Configuration of read / write mode

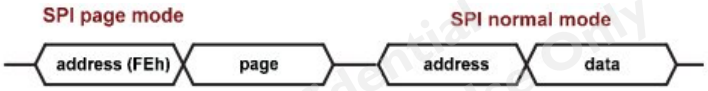
Reg NO.		Reg Data	Description
Dec	Hex	Page	
R253	RFD	XXh	When the accessed command is FD00h, all registers of page 00 are set to write condition.
R254	RFE	XXh	When the accessed command is FE00h, all registers of page 00 are set to read condition.

SPI write mode



cmd run	Cmd parameter		Register Parameter		
			Page	Page address	Write Data
0	Address	Data			
1	FDh	00h	→ 00	N/A	N/A
2	04h	A8h	00	→ 0004	A8
3	05h	0Bh	00	→ 0005	0B
4	FDh	D1h	→ D1	N/A	N/A
5	01h	30h	D1	→ D101	30
6	02h	11h	D1	→ D102	11

SPI read mode



cmd run	Cmd parameter		Register Parameter		
			Page	Page address	Read Data
0	Address	Data			
1	FEh	00h	→ 00	N/A	N/A
2	04h		00	→ 0004	A8
3	05h		00	→ 0005	0B
4	FEh	D1h	→ D1	N/A	N/A
5	01h		D1	→ D101	30
6	02h		D1	→ D102	11

6.4 Register table

Page Address	Register Data								Default
Hex	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0001	0	0	0	0	0	0	0	STB	8'h00
0002	0	0	0	RESX	0	0	0	0	8'h10
0004	0	Cb_Cr	16_Y_CbCr	0	YUV_ Matrix[1]	YUV_ Matrix[0]	UV_INTERP OLATION	YUV_ OFFSET	8'h40
0006	0	0	0	0	0	CONTRAST _G8	CONTRAST _G8	CONTRAST _B8	8'h07
0007	CONTRAST _R[7]	CONTRAST _R[6]	CONTRAST _R[5]	CONTRAST _R[4]	CONTRAST _R[3]	CONTRAST _R[2]	CONTRAST _R[1]	CONTRAST _R[0]	8'h40
0008	CONTRAST _G[7]	CONTRAST _G[6]	CONTRAST _G[5]	CONTRAST _G[4]	CONTRAST _G[3]	CONTRAST _G[2]	CONTRAST _G[1]	CONTRAST _G[0]	8'h40
0009	CONTRAST _B[7]	CONTRAST _B[6]	CONTRAST _B[5]	CONTRAST _B[4]	CONTRAST _B[3]	CONTRAST _B[2]	CONTRAST _B[1]	CONTRAST _B[0]	8'h40
000C	0	0	0	0	0	0	0	CONTRAST _SET	8'h00
000D	Brightness_ R[7]	Brightness_ R[6]	Brightness_ R[5]	Brightness_ R[4]	Brightness_ R[3]	Brightness_ R[2]	Brightness_ R[1]	Brightness_ R[0]	8'h40
000E	Brightness_ G[7]	Brightness_ G[6]	Brightness_ G[5]	Brightness_ G[4]	Brightness_ G[3]	Brightness_ G[2]	Brightness_ G[1]	Brightness_ G[0]	8'h40
000F	Brightness_ B[7]	Brightness_ B[6]	Brightness_ B[5]	Brightness_ B[4]	Brightness_ B[3]	Brightness_ B[2]	Brightness_ B[1]	Brightness_ B[0]	8'h40
0018	0	0	0	0	0	0	0	INTF_IM	8'h00
0019	HBLK_EN	0	0	VBLK[4]	VBLK[3]	VBLK[2]	VBLK[1]	VBLK[0]	8'h15
001A	HBLK[7]	HBLK[6]	HBLK[5]	HBLK[4]	HBLK[3]	HBLK[2]	HBLK[1]	HBLK[0]	8'h51
001C	0	0	0	0	0	0	VDIR	HDIR	8'h03

R01h Software standby mode setting

No	Register address								MSB Register data							LSB
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
01h	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	STB

-R01h[0] STB：Standby(power saving) mode setting

STB	Function
0	**Standby; timing control, DAC, and DC/DC converter are off, and register data should be kept. (Default)**
1	Normal operation, with power on/off sequence

R02h Software reset mode setting

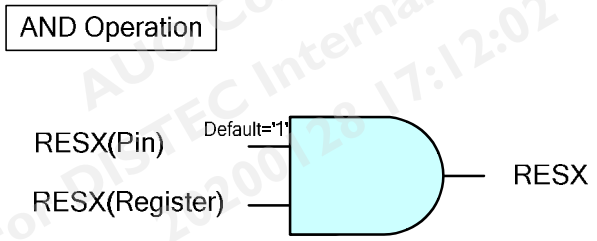
No	Register address								MSB Register data							LSB
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
02h	0	0	0	0	0	0	1	0	0	0	0	RESX	0	0	0	0

-R02h[4] RESX : Register reset setting

RESX	Function
0	Reset all registers to default value
1	**Normal operation (Default)**

Note : When this command is sent to ASIC, it will be executed immediately.

Note : Relationship between Pin and Register. If the pin (register) is set to '1', the RESX function will be decided by the register (pin) setting fully.



R04h YUV format setting (For YUV mode)

No	Register address								MSB	Register data						LSB
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
04h	0	0	0	0	0	1	0	0	0	Cb_Cr	16_Y_ CbCr	0	YUV_ Matrix[1]	YUV_ Matrix[0]	UV_INT ERPOLA TION	YUV_ OFFSET

Note : When R18 INTF_IM = 1

-R04h[6] Cb_Cr : Cb and Cr position exchange

-R04h[5] 16_Y_CbCr : Y and CbCr position exchange

16_Y_CbCr	Cb_Cr											
	R04h[6] = 0							R04h[6] = 1(Default)						
0(Default)	DR[7:0]	Cr1	Cb1	Cr2	Cb2	Cr3	Cb3	DR[7:0]	Cb1	Cr1	Cb2	Cr2	Cb3	Cr3
	DG[7:0]	Y1	Y2	Y3	Y4	Y5	Y6	DG[7:0]	Y1	Y2	Y3	Y4	Y5	Y6
1	DR[7:0]	Y1	Y2	Y3	Y4	Y5	Y6	DR[7:0]	Y1	Y2	Y3	Y4	Y5	Y6
	DG[7:0]	Cr1	Cb1	Cr2	Cb2	Cr3	Cb3	DG[7:0]	Cb1	Cr1	Cb2	Cr2	Cb3	Cr3

-R04h[3:2] YUV_Matrix : YUV color space transform formula selection

-R04h[0] YUV_OFFSET : Cb and Cr signed / unsigned format selection

YUV_Matrix	YUV_OFFSET	
	R04h[0] = 0(Default)	R04h[0] = 1
00(Default)	Matrix A R=Y + 1.402xCr G=Y – 0.344xCb – 0.714xCr B=Y + 1.772xCb Where Y=0~255 Cb&Cr=-128~127	Matrix A R=Y+1.402x(Cr-128) G=Y-0.344x(Cb-128)-0.714x(Cr-128) B=Y+1.772x(Cb-128) Where Y=0~255 Cb&Cr=0~255
01	Matrix B R=1.164x(Y-16) + 1.596xCr G=1.164x(Y-16) – 0.813xCr – 0.391xCb B=1.164x(Y-16) + 2.018xCb Where Y=16~235 Cb&Cr=-112~112	Matrix B R=1.164x(Y-16)+1.596x(Cr-128) G=1.164x(Y-16)–0.813x(Cr-128)-0.391x(Cb-128) B=1.164x(Y-16)+2.018x(Cb-128) Where Y=16~235 Cb&Cr=16~240
10	Matrix C R=Y + 1.371xCr G=Y – 0.336xCb – 0.698xCr B=Y + 1.732xCb Where Y=0~255 Cb&Cr=-128~127	Matrix C R=Y+1.371x(Cr-128) G=Y-0.336x(Cb-128)-0.698x(Cr-128) B=Y+1.732x(Cb-128) Where Y=0~255 Cb&Cr=0~255
11	Reserved	Reserved

-R04h[1] UV_INTERPOLATION : Cb and Cr interpolation mode setting

UV_INTERPOLATION	Function
0(Default)	Y1 Y2 Y3 Y4 Y5 Cb1 Cb1 Cb3 Cb3 Cb5 Cr1 Cr1 Cr3 Cr3 Cr5
1	Y1 Y2 Y3 Y4 Y5 Cb1 (Cb1+Cb3) / 2 Cb3 (Cb3+Cb5) / 2 Cb5 Cr1 (Cr1+Cr3) / 2 Cr3 (Cr3+Cr5) / 2 Cr5

Note : When UV_INTERPOLATION = 1, Cb2n = (Cb(2n-1) + Cb(2n+1)) / 2, Cr2n = (Cr(2n-1) + Cr(2n+1)) / 2

-R04h[0] YUV_OFFSET : Cb and Cr signed/unsigned format selection

YUV_OFFSET	Function
0(Default)	Cb & Cr are signed number Matrix A -128~127 Matrix B -112~112 Matrix C -128~127
1	Cb & Cr are unsigned number Matrix A 0~255 Matrix B 16~240 Matrix C 0~255

R06h~R0Bh RGB Contrast level setting

No	Register address								MSB Register data							LSB
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
06h	0	0	0	0	0	1	1	0	0	0	0	0	0	CONTRAST_R8	CONTRAST_G8	CONTRAST_B8
07h	0	0	0	0	0	1	1	1	CONTRAST_R[7:0]							
08h	0	0	0	0	1	0	0	0	CONTRAST_G[7:0]							
09h	0	0	0	0	1	0	0	1	CONTRAST_B[7:0]							

Type1: CONTRAST_R8/G8/B8 = 0, (1 / 512) / bit

CONTRAST_R8/G8/B8	CONTRAST_R/G/B[7:0]	Contrast gain
0	00h	0.500
0	01h	0.502
0	80h	0.750
0	FEh	0.996
0	FFh	0.998

Type2: CONTRAST_R8/G8/B8 = 1, (1 / 64) / bit

CONTRAST_R8/G8/B8	CONTRAST_R/G/B[7:0]	Contrast gain
1	00h	0.000
1	01h	0.016
1 (Default)	40h (Default)	1.000 (Default)
1	FEh	3.969
1	FFh	3.984

R0Ch Contrast enable setting

No	Register address								MSB Register data							LSB
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0Ch	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	CONTRAST_SET

-R0Ch[0] CONTRAST_SET : Contrast gain setting enable

CONTRAST_SET	Function
0(Default)	**Contrast gain setting disable**
1	Contrast gain setting enable

R0Dh/R0Eh/R0Fh RGB Brightness level setting

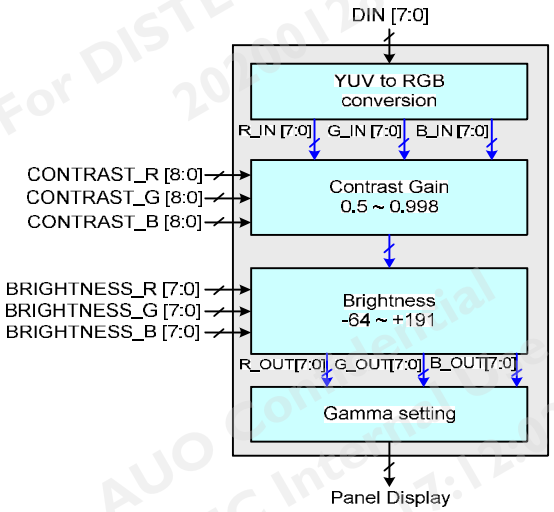
No	Register address								MSB Register data							LSB
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0Dh	0	0	0	0	1	1	0	1	Brightness_R[7:0]							
0Eh	0	0	0	0	1	1	1	0	Brightness_G[7:0]							
0Fh	0	0	0	0	1	1	1	1	Brightness_B[7:0]							

-R0Dh Brightness_R : R bright level setting, setting accuracy：1 step / bit

-R0Eh Brightness_G : G bright level setting, setting accuracy：1 step / bit

-R0Fh Brightness_B : B bright level setting, setting accuracy：1 step / bit

Brightness_R/G/B[7:0]	Brightness gain
00h	Dark(-64)
40h(Default)	**Center (0) (Default)**
FFh	Bright (+191)



- R_OUT = R_IN x CONTRAST_R + BRIGHTNESS_R
- G_OUT = G_IN x CONTRAST_G + BRIGHTNESS_G
- B_OUT = B_IN x CONTRAST_B + BRIGHTNESS_B

Note：Output values below “0” and above “255” are clipped.

R18h Interface setting

No	Register address								MSB Register data LSB							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
18h	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	INTF_IM

-R18h[0] Interface setting

INTF_IM	Function
0h (Default)	**RGB 24-bit (Default)**
1h	YUV 16-bit

R19h/R1Ah Blanking setting

No	Register address								MSB Register data LSB							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
19h	0	0	0	1	1	0	0	1	HBLK_EN	0	0	VBLK[4:0]				
1Ah	0	0	0	1	1	0	1	0	HBLK[7:0]							

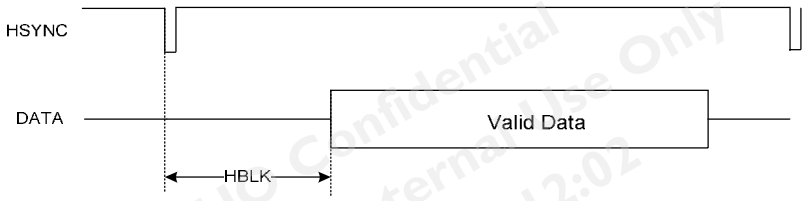
-R19h[4:0] VBLK : Vertical blanking setting：

VBLK		Unit	Remark
HEX	DEC		
01h	1	HSYNC	
15h (Default)	**21 (Default)**		
1Fh	31		

-R19h[7] & R1Ah[7:0] HBLK_EN & HBLK：Horizontal blanking setting

HBLK_EN	HBLK		Unit	Remark
	HEX	DEC		
1	01h	1	DCLK	
	51h	81		
	FFh	255		
0 (Default)	**28h (Fixed)**	**40**		

Note : The frequency of DCLK is different under different input timing.



R1Ch Scan shift direction setting

No	Register address								MSB Register data							LSB
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
1Ch	0	0	0	1	1	1	0	0	0	0	0	0	0	0	VDIR	HDIR

-R1Ch[1] VDIR: Vertical shift direction setting

VDIR	Function
0	Shift from down to up, Last line = L1←L2…L1439←L1440 = First line
1(Default)	**Shift from up to down, First line = L1→L2…L1439→L1440 = Last line (Default)**

-R1Ch[0] HDIR: Horizontal shift direction setting

HDIR	Function
0	Shift from right to left, Last data = D1←D2…D639←D640 = First data
1(Default)	**Shift from left to right, First data = D1→D2…D639→D640 = Last data (Default)**

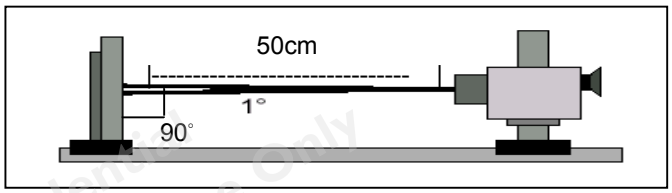
C. Optical specification (Refer to Note 1, Note 2, Note 3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time							Note 4
Rise	Tr	θ =0°	-	18	36	ms	
Fall	Tf		-	18	36	ms	
Contrast ratio	CR	At optimized viewing angle	700	1000	-		Note 5
Viewing angle							Note 6
Top	φ_T	CR≧100	70	85	-	deg.	
Bottom	φ_B		70	85	-		
Left	φ_L		70	85	-		
Right	φ_R		70	85	-		
Brightness * (20mA)	Y_L	θ =0°	440	550	-	cd/m^2	Note 7
Luminance Uniformity			75	80		%	Note 8
Color Chromaticity	Wx	θ =0°	0.260	0.310	0.360		
	Wy	θ =0°	0.280	0.330	0.380		
	Rx	θ =0°	0.590	0.640	0.690		
	Ry	θ =0°	0.280	0.330	0.380		
	Gx	θ =0°	0.250	0.300	0.350		
	Gy	θ =0°	0.550	0.600	0.650		
	Bx	θ =0°	0.100	0.150	0.200		
	By	θ =0°	0.010	0.060	0.110		

Note 1. Ambient temperature =25℃.

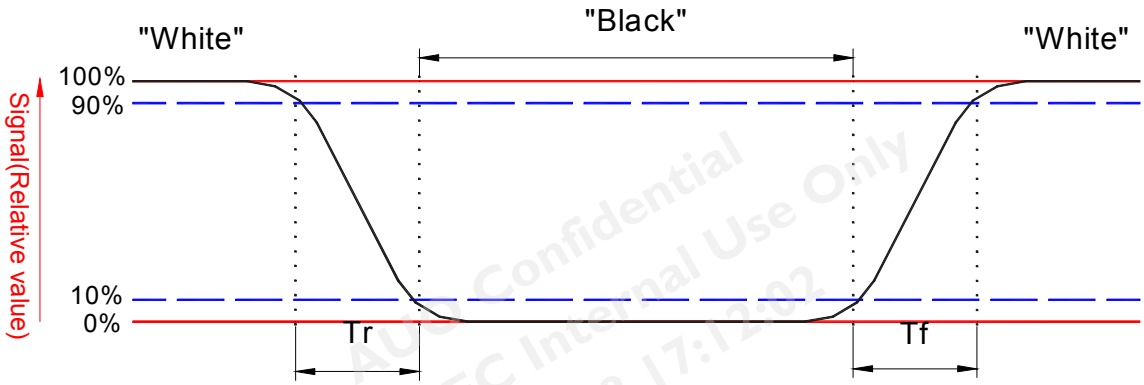
Note 2.To be measured in the dark room.

Note 3.To be measured on the center area of panel with a field angle of 1° by Topcon luminance meter BM-5A, after 10 minutes operation.



Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



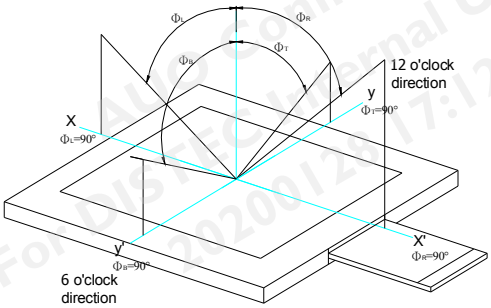
Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. Definition of viewing angle:

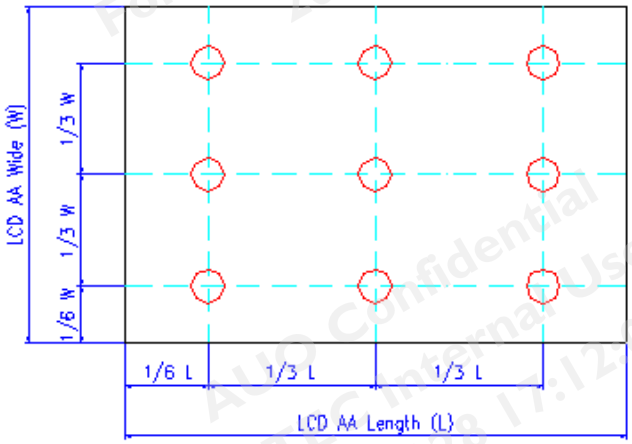
Refer to figure as below.



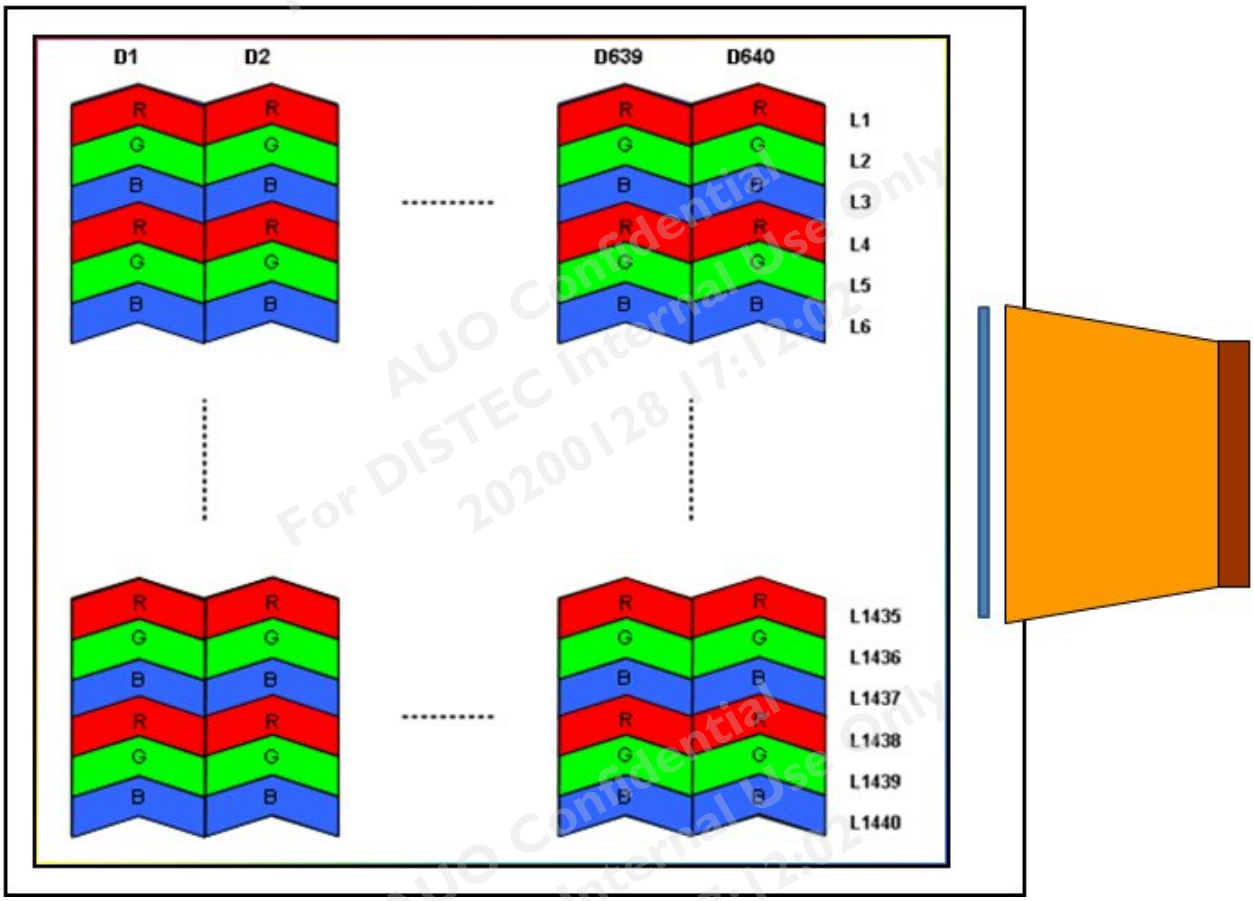
Note 7. Measured at the center area of the panel in white pattern based on 3,4 Backlight driving conditions to setup LED current.

Note 8. Definition of luminance uniformity

$$\text{Luminance Uniformity} = \frac{\text{Min. Brightness of nine point}}{\text{Max. Brightness of nine point}}$$



Note 9. Color Filter Arrangement



D. Reliability test items (Refer to Note 1, Note 2, Note 3)

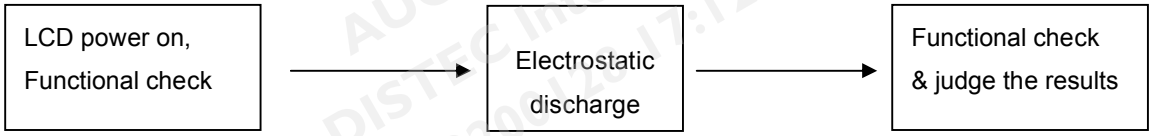
No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 70℃ 240Hrs	
2	Low temperature storage	Ta= -30℃ 240Hrs	
3	High temperature operation	Ta= 60℃ 240Hrs	
4	Low temperature operation	Ta= -10℃ 240Hrs	
5	High temperature and high humidity	Ta= 60℃. 90% RH 240Hrs	Operation
6	Heat shock	-25℃~80℃/50 cycle, 2Hrs/cycle	Non-operation
7	Electrostatic discharge	Air-mode : +/- 8kV Contact-mode : +/- 4kV	Note.4 Note 5
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
9	Mechanical shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
10	Vibration (with carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 75cm 1 corner, 3 edges, 6 surfaces	

Note 1. (for test item 1 to 6) Ta: Ambient temperature

Note 2. (for test item 1 to 6) Test method: check with recovery time 2hrs in the laboratory environment

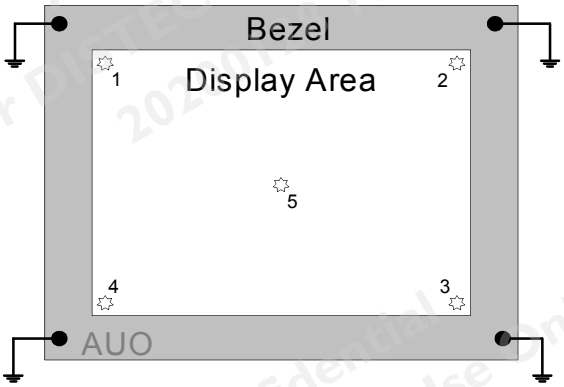
Note 3. Judged by the on/off testing results of AUO's standard w/o functional fail.

Note 4. ESD Testing Flow as the below



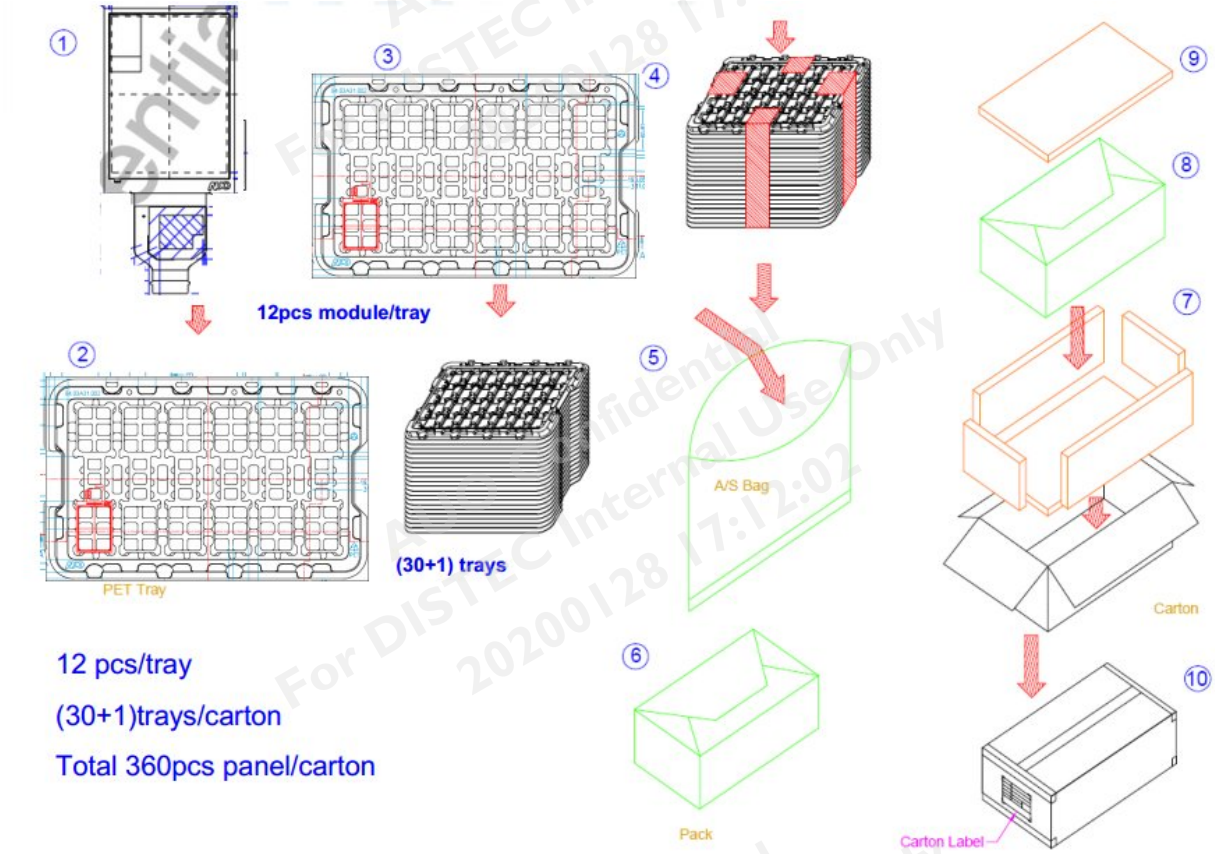
Note 5. ESD testing method.

1. Ambient: 24~26℃, 56~65%RH
2. Instruments:NoisekenESS-2000,
3. Test Mode: Operating mode, test pattern: colorbar+8Gray scale
4. Test Method:
   a. Contact Discharge:, 150pF(330Ω) 1sec, 5 points, 10 times/point
   b. Air Discharge:, 150pF(330Ω) 1sec, 5 points, 10 times/point
5. Test point:



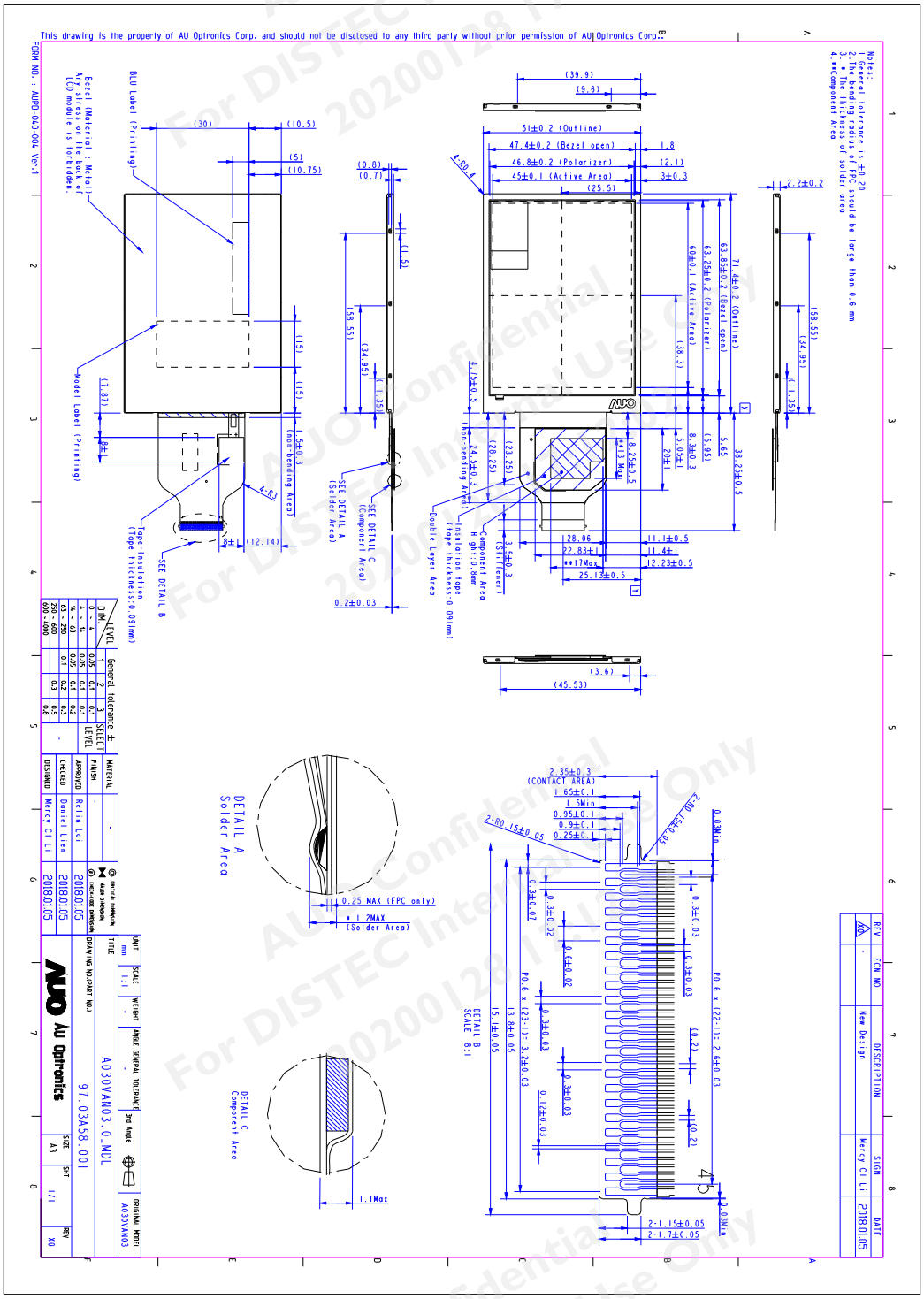
6. The metal casing is connected to power supply ground (0V) at four corners.
7. All register commands are repeating transfer.

E. Packing form



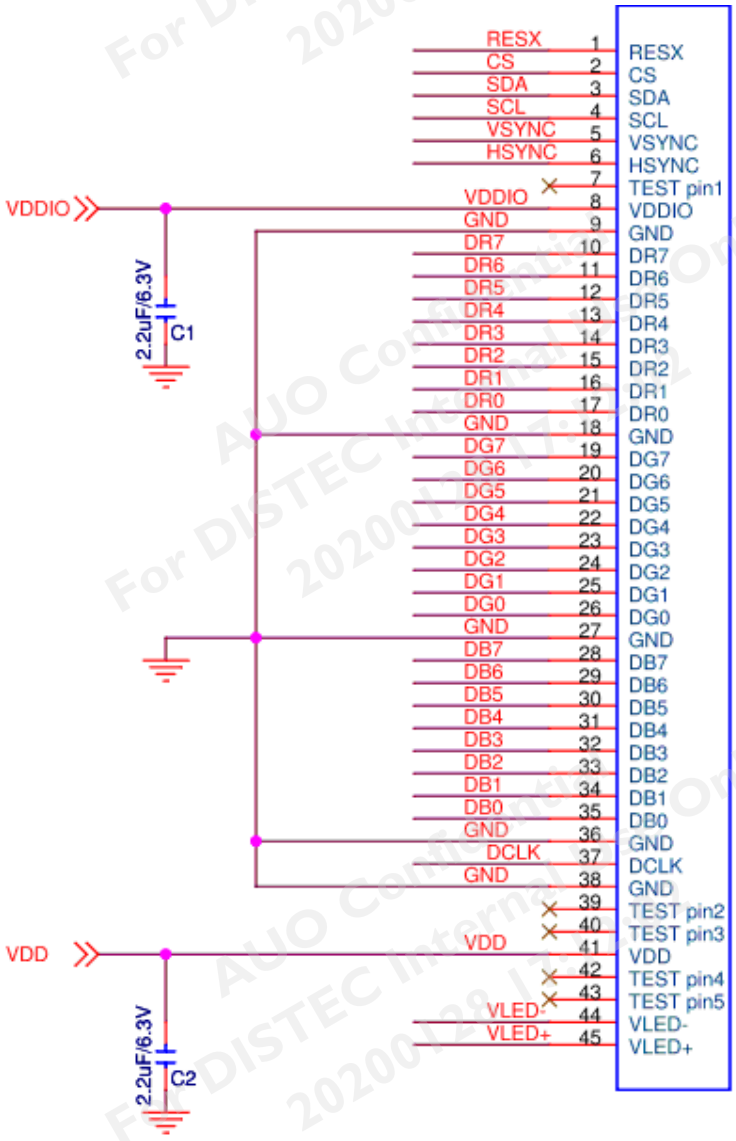
1	2	3	4	5	6	7	8	9	10	11	12
0	7	2	8	S	0	6	Z	1	9	0	1
Month		Date		Module FAB			Grade	Serial Number		Part. Number	

F. Outline dimension



G. Application note

1. Application circuit

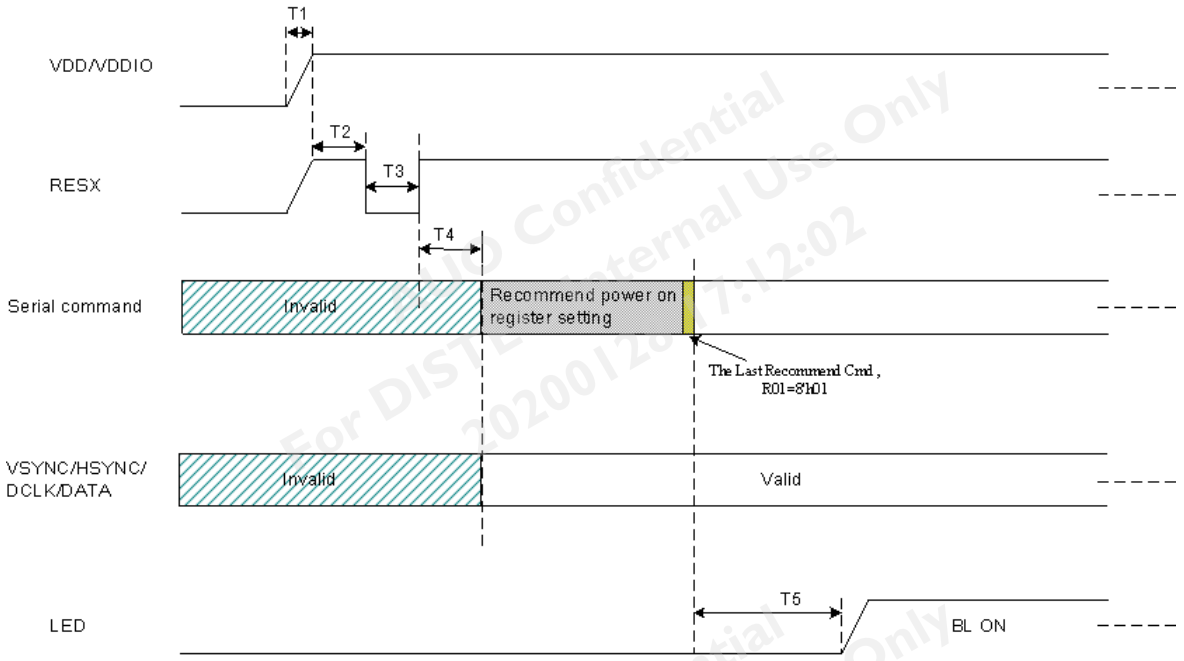


2. Power on/off sequence

2.1 Power on

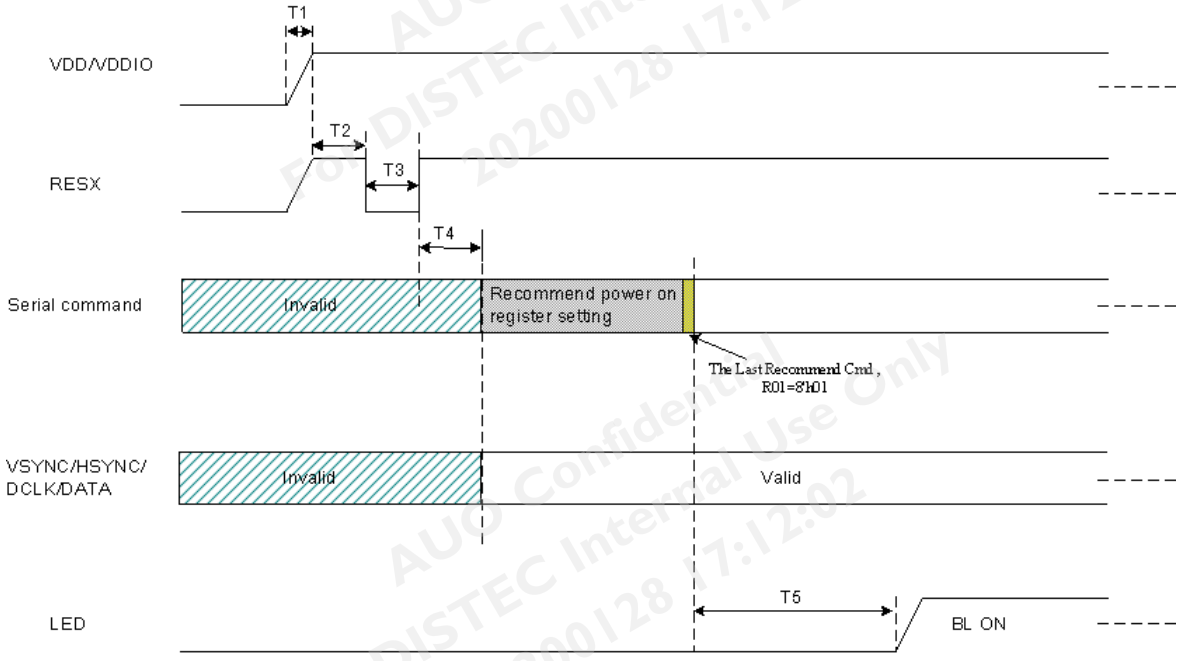
After VDD power on, VSYNC/HSYNC/DCLK/DATA can be input, and serial peripheral interface is also operational. The LCD driver is in default standby mode after VDD power-on, and setting register STB to '1' to disable the standby mode is required for normal operation. When the standby mode is disabled, a build-in power on sequence is started.

Frame rate: 60Hz



T1> 10 us, T2> 1 ms, T3> 3 ms, T4> 10 ms, T5> 85 ms

Frame rate: 50Hz

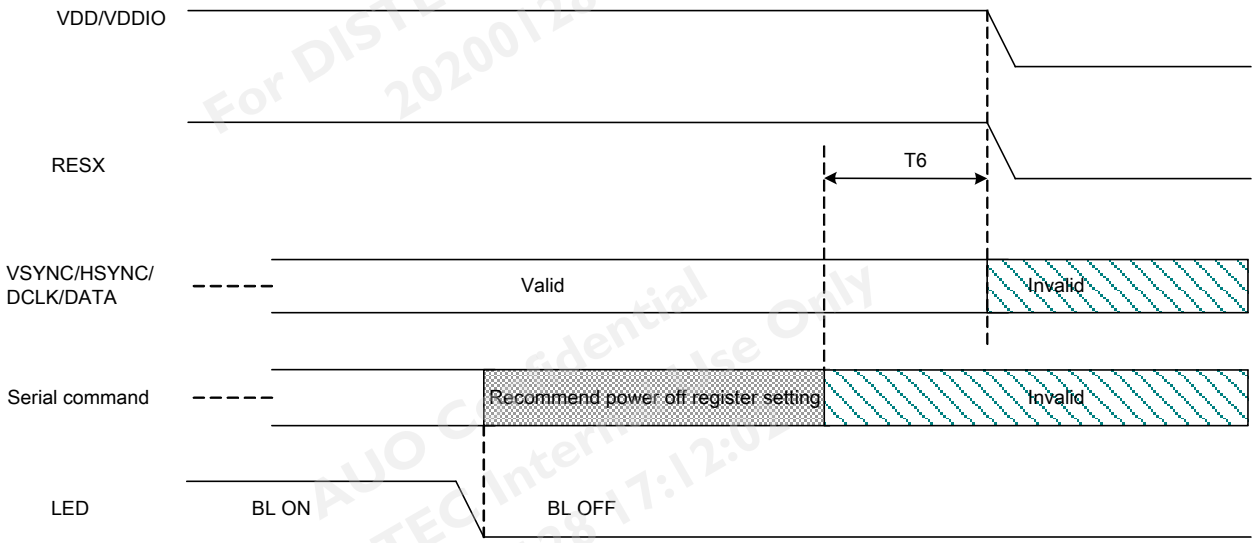


T1> 10 us, T2> 1 ms, T3> 3 ms, T4> 10 ms, T5> 100 ms

2.2 Power off

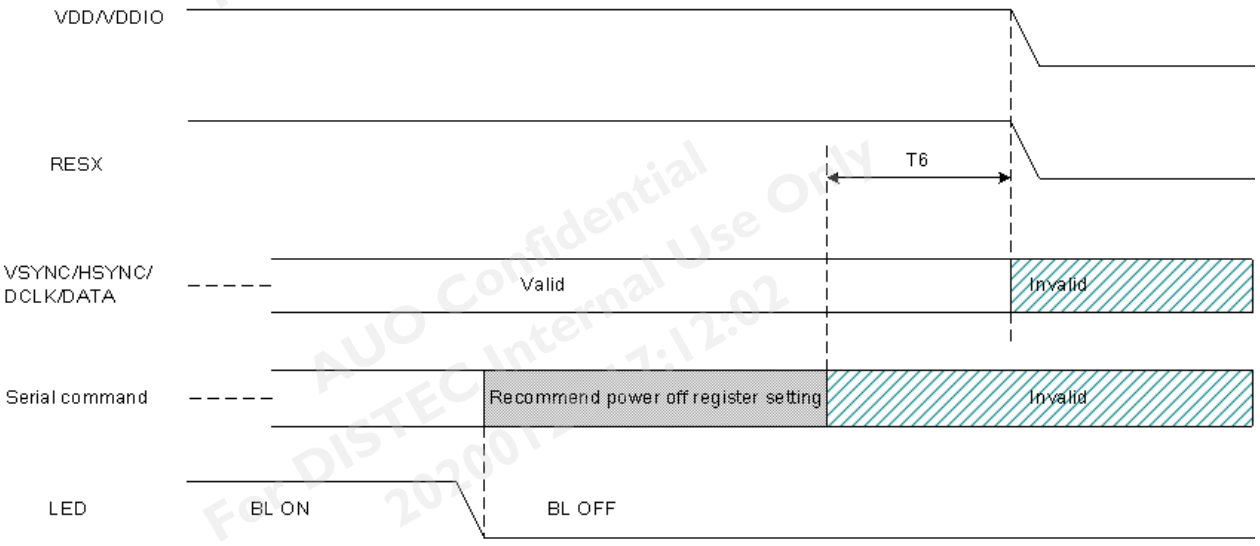
When the register STB is set to '0' to enable standby mode, a build-in power off sequence is started.

Frame rate: 60Hz



T6> 67 ms

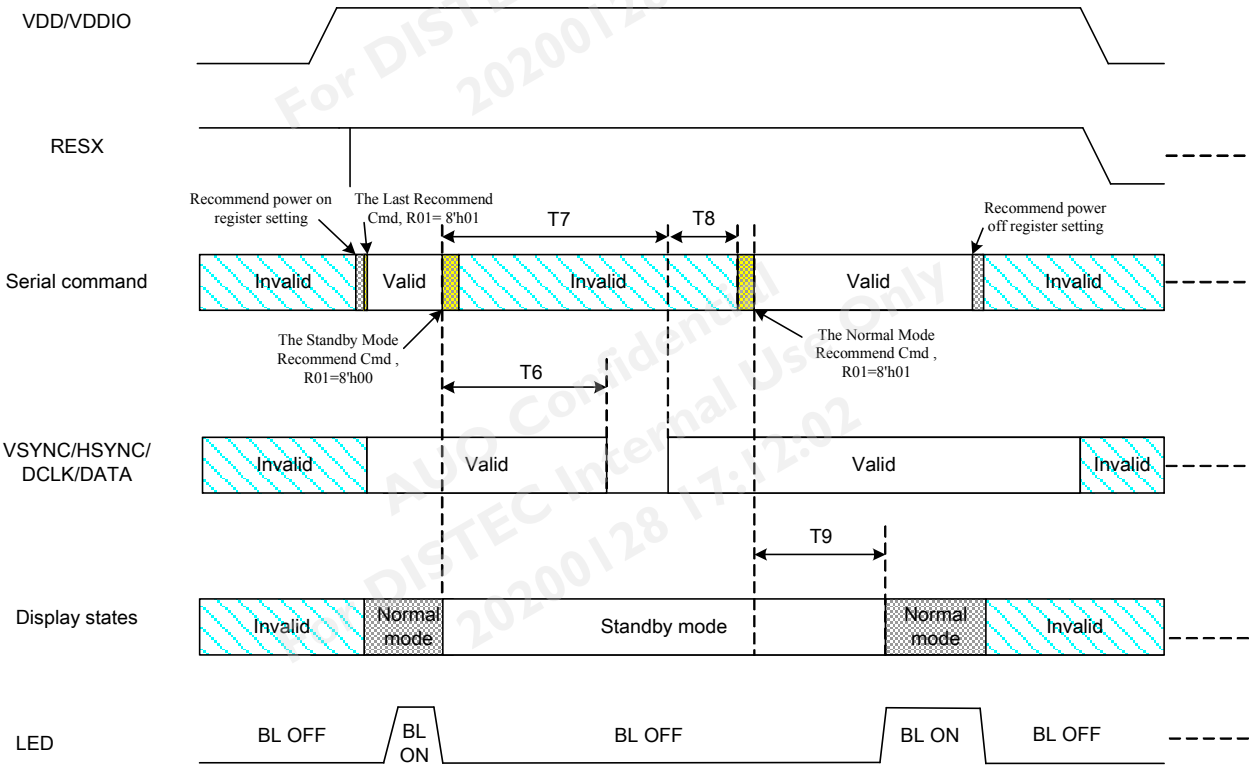
Frame rate: 50Hz



T6> 80 ms

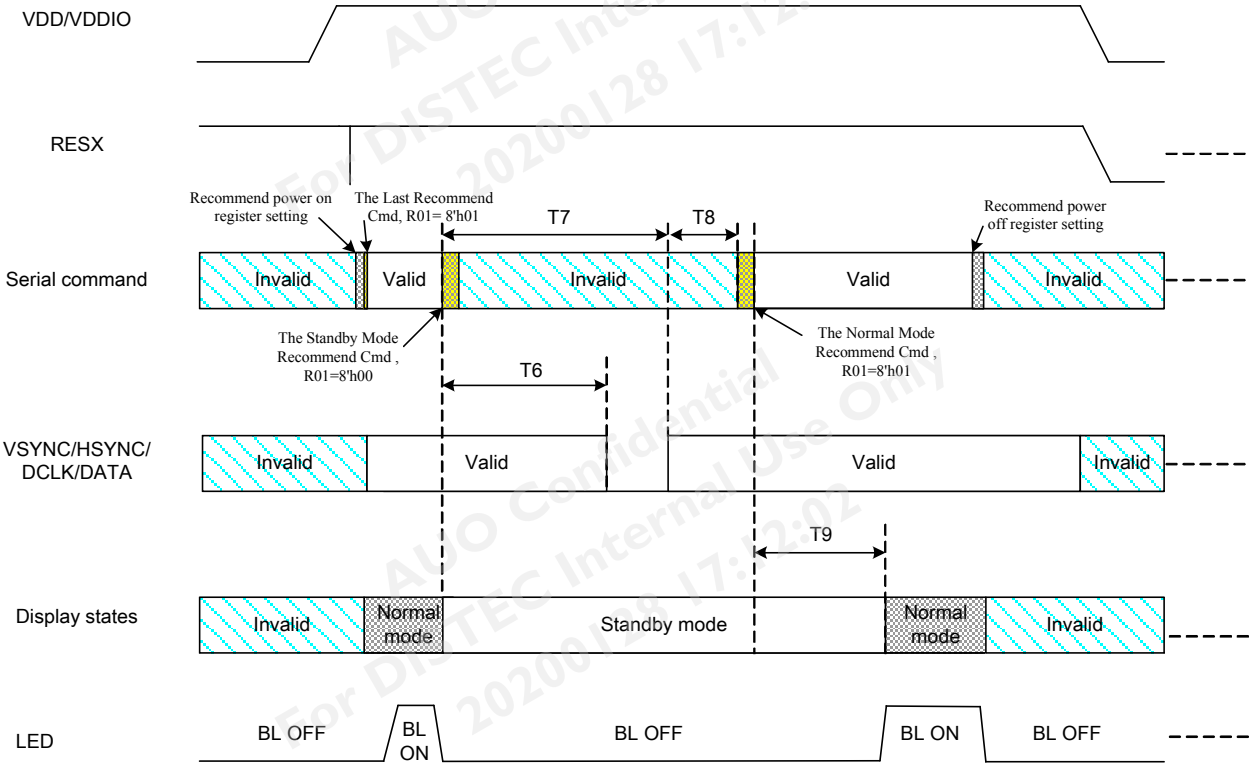
2.3 Standby mode on/off

Frame rate: 60Hz



T6 > 67ms, T7> 100 ms, T8> 1 ms, T9 > 85ms

Frame rate: 50Hz



T6 > 80ms, T7> 120 ms, T8> 1 ms, T9 > 100ms

3. Recommended power on/off serial command settings

a. Recommended Power On Register Setting (For YUV-16bit mode)

Number	Address	Data	Description	Remark
Signal input start(VS/HS/DCLK)				
1	FDh	FFh		
2	81h	56h		
3	82h	01h		
4	FDh	00h		
5	18h	01h	YUV 16-bit format	
6	19h	95h	VBLK	Note 1
7	1Ah	28h	HBLK	Note 2
8	FDh	D8h		
9	01h	21h		
10	02h	21h		
11	FDh	E1h		
12	01h	5Fh		
13	02h	0Dh		
14	03h	21h		
15	04h	2Fh		
16	05h	10h		
17	06h	11h		
18	07h	21h		
19	08h	08h		
20	09h	08h		
21	0Ah	08h		
22	0Bh	0Bh		
23	0Ch	13h		
24	0Dh	10h		
25	0Eh	0Fh		
26	0Fh	14h		
27	10h	0Bh		
28	11h	02h		
29	12h	07h		
30	FDh	E2h		
31	01h	79h		
32	02h	0Dh		
33	03h	21h		

34	04h	2Fh		
35	05h	10h		
36	06h	11h		
37	07h	21h		
38	08h	08h		
39	09h	08h		
40	0Ah	08h		
41	0Bh	0Bh		
42	0Ch	13h		
43	0Dh	10h		
44	0Eh	0Fh		
45	0Fh	14h		
46	10h	0Bh		
47	11h	02h		
48	12h	07h		
49	FDh	E3h		
50	01h	0Fh		
51	02h	02h		
52	03h	08h		
53	04h	0Eh		
54	05h	0Ch		
55	06h	0Dh		
56	07h	14h		
57	08h	06h		
58	09h	05h		
59	0Ah	0Bh		
60	0Bh	0Ch		
61	0Ch	1Ah		
62	0Dh	10h		
63	0Eh	0Eh		
64	0Fh	1Bh		
65	10h	0Eh		
66	11h	02h		
67	12h	07h		
68	FDh	E4h		
69	01h	23h		
70	02h	02h		

71	03h	08h		
72	04h	0Eh		
73	05h	0Ch		
74	06h	0Dh		
75	07h	14h		
76	08h	06h		
77	09h	05h		
78	0Ah	0Bh		
79	0Bh	0Ch		
80	0Ch	1Ah		
81	0Dh	10h		
82	0Eh	0Eh		
83	0Fh	1Bh		
84	10h	0Eh		
85	11h	03h		
86	12h	07h		
87	FDh	E5h		
88	01h	19h		
89	02h	02h		
90	03h	09h		
91	04h	11h		
92	05h	0Ch		
93	06h	0Eh		
94	07h	11h		
95	08h	06h		
96	09h	06h		
97	0Ah	0Ah		
98	0Bh	0Ch		
99	0Ch	25h		
100	0Dh	14h		
101	0Eh	19h		
102	0Fh	04h		
103	10h	03h		
104	11h	02h		
105	12h	07h		
106	FDh	E6h		
107	01h	2Fh		

108	02h	02h		
109	03h	09h		
110	04h	11h		
111	05h	0Ch		
112	06h	0Eh		
113	07h	11h		
114	08h	06h		
115	09h	06h		
116	0Ah	0Ah		
117	0Bh	0Ch		
118	0Ch	25h		
119	0Dh	14h		
120	0Eh	19h		
121	0Fh	04h		
122	10h	03h		
123	11h	02h		
124	12h	07h		
125	FDh	C4h		
126	82h	05h		
127	FDh	C1h		
128	91h	43h		
129	FDh	C0h		
130	A1h	01h		
131	A2h	1Ch		
132	A3h	0Ah		
133	A4h	34h		
134	A5h	00h		
135	A6h	09h		
136	A7h	34h		
137	A8h	00h		
138	A9h	09h		
139	AAh	34h		
140	FDh	CEh		
141	81h	14h		
142	82h	3Eh		
143	83h	3Eh		
144	91h	07h		

145	93h	31h		
146	94h	02h		
147	95h	07h		
148	97h	31h		
149	98h	02h		
150	99h	07h		
151	9Bh	31h		
152	9Ch	02h		
153	FDh	00h		
154	01h	01h	standby mode disable	
WAIT >10ms				
Others command				

Note 1: V-blanking must be adjusted based on the command.

Note 2: H-blanking must be adjusted based on the command.

b. Recommended Power Off Register Setting

Number	Address	Data	Description
1	01h	00h	standby mode enable

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