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Datasheet

Ortustech

COM32H3P68ULC

OR-20-033

July 21, 2020

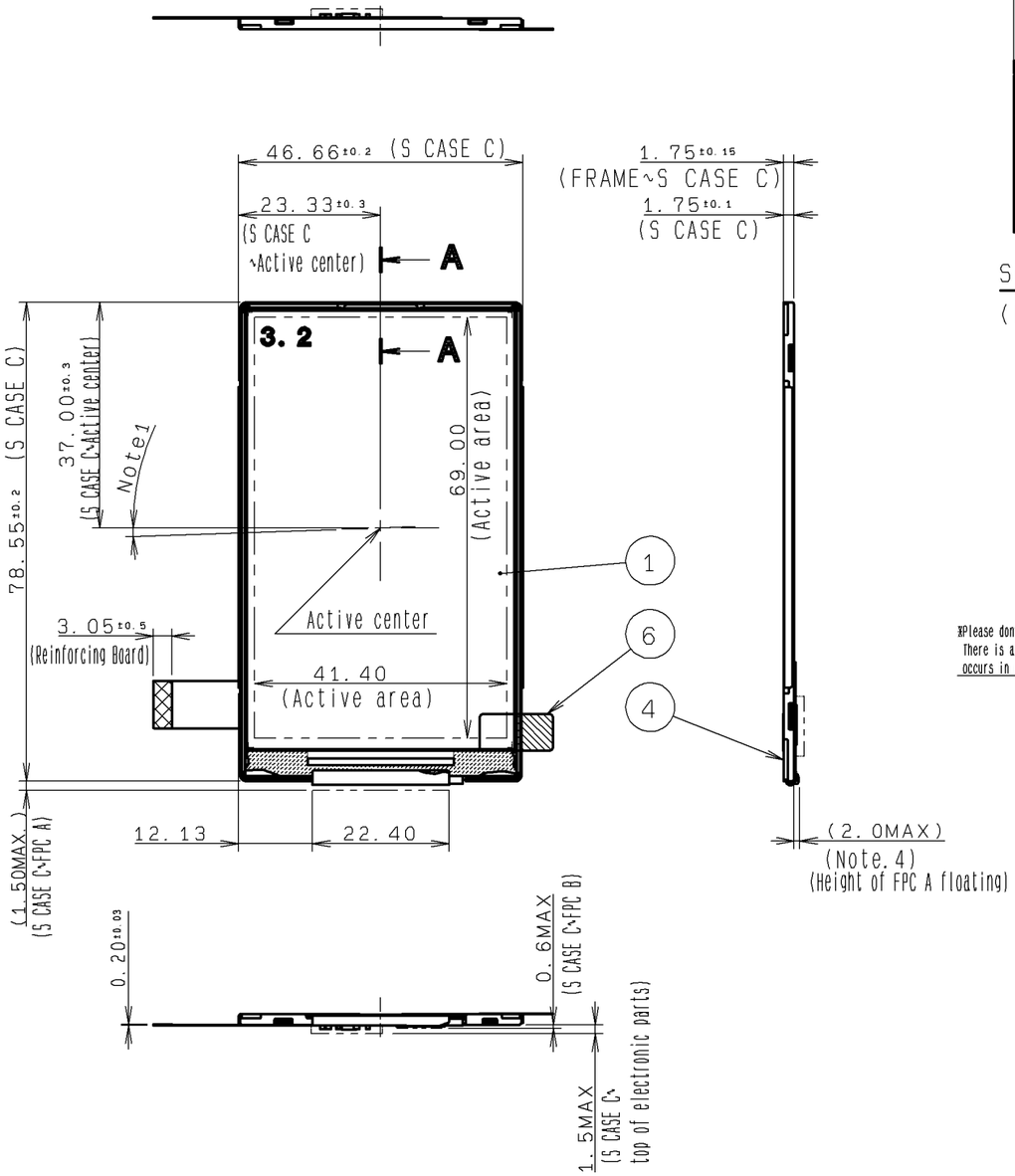
Preliminary Information of COM32H3P68ULC Specifications

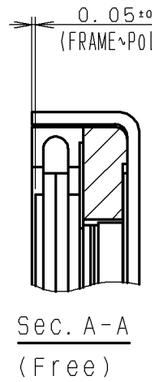
This is “preliminary” information of new product “COM32H3P68ULC”. Formal Product Specifications is supposed to issued within a couple of months. Please note that final specification values may change from this preliminary technical information.

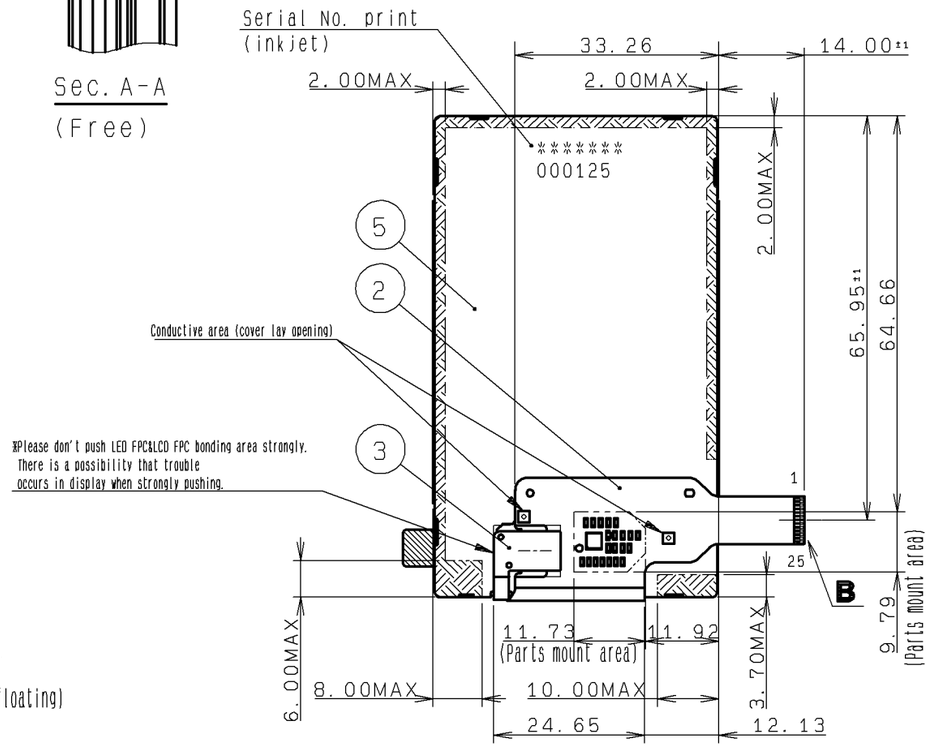
3.2 Outward Form

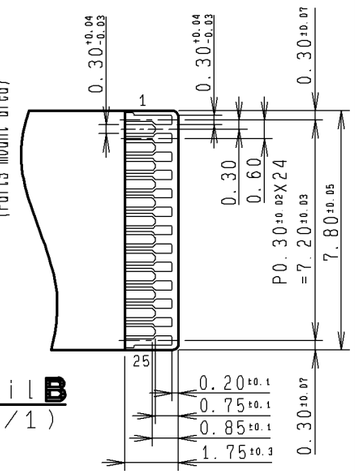
EC No.	REV. No.	REVISE	DATE (Y:M:D)	APPROVED	CHECKED	PREPARED

(8/42)
19TLM088
Issue:Jan.23,2020









Note 1. Angular deviation of LCD cell from the TFT-LCD monitor's reference axis shall be less than 【±40'】.

Note 2. Protective film is affixed on front surface of the screen.
Location tolerance of the protective film shall be ±1.5 mm to the polarizing film.

Note 3. In order to realize thin module structure, double-sided adhesive tapes are used to fix LCD panels.
As these tapes do not guarantee to permanently fix the panels,
LCD panel may rize from the module when shiped from factory.
So please make sure to design the system to hold the edges of LCD panel
by the soft material such as sponge when LCD module is assembled into the cabinet.

Note 4. In order to realize thin module structure, double-sided adhesive tapes are used to fix FPC at S CASE C. As these tapes do not guarantee to permanently fix the FPC near the bending area, FPC may rize from the module when shiped from factory.

Note 5. In case TFT-LCD monitor is fixed to the case of your product, it's recommended that monitor is fixed in to ▨ area.

Note 6. Recommended FPC connector.
For FPC A:HRS FH35C-25S-0.3SHW

PART NAME	ITEM	PART CODE	MODEL NUMBER	REMARK
	7			
R TAPE	6			
S CASE C	5		SUS(t=0.2)	
FRAME	4		PC	
FPC B	3			Use of LED
FPC A	2			Use of LCD
TFT-LCD PANEL	1		Glass thickness=0.2t+0.2t	

APPROVED 尾木	GENERAL TOLERANCE ±0.5	SCALE 1/1	UNIT mm	TOPPAN PRINTING CO., LTD.
CHECKED 加藤	ISSUE (Y:M:D) 20:01:23	MODEL [redacted]		DO NOT DUPLICATE, CONFIDENTIAL AND PROPRIETARY
CHECKED	NAME			DRAWING NO. [redacted] REV. SHEET DIV.
DESIGN 増田剛	[redacted] OUTLINE D3P61			ASS'Y
DRAW 増田剛				

2. Outline Specifications

2.1 Features of the Product

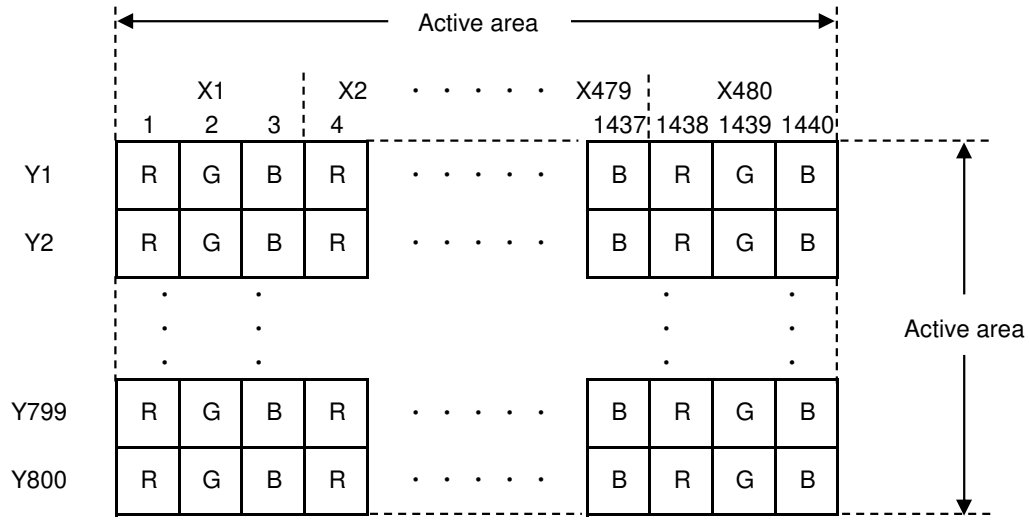
- 3.2 inch diagonal display, 480 x RGB [H] x 800 [V] dots.
- 24bitRGB (8-8-8 Format) / 16.7 Million colors.
- MIPI DSI as high-speed interface. Video mode only.
- Timing generator [TG], Counter-electrode driving circuitry, Built-in power supply circuit.
- Various display controls and functional selection.
- High bright white LED back-light.
- Blanview TFT-LCD, improved outdoor readability.

* MIPI : Mobile Industrial Processor Interface , DSI : Display Serial Interface

	Indoor		Outdoor	
	Readability	Power Efficiency (Battery Life)	Readability	Power Efficiency (Battery Life)
Transmissive	Good	Good	Fair	Poor
Transflective	Fair	Poor	Good	Good
Blanview	Good	Good	Good	Good

2.2 Display Method

Items	Specifications	Remarks
Display type	VA 16.7 Million colors. Blanview, Normally black.	
Driving method	a-Si TFT Active matrix. Line-scanning, Non-interlace.	
Dot arrangement	RGB stripe arrangement.	Refer to "Dot arrangement"
Signal input method	MIPI DSI 2-lanes : 2 data lanes and 1 clock lane	
Backlight type	High bright white LED.	
NTSC ratio	35%	



Dot arrangement

3. Dimensions and Shape

3.1 Dimensions

Items	Specifications	Unit	Remarks
Outline dimensions	46.66[H] × 78.55[V] ×1.75[D]	mm	Exclude FPC cable and parts on FPC
Active area	41.40[H] × 69.00[V]	mm	
Number of dots	1440[H] × 800[V]	dot	
Dot pitch	28.75[H] × 86.25[V]	um	
Surface hardness of the polarizer	3	H	Load: 2.0 N
Weight	14.7	g	Include FPC cable

Ⓐ 4. Pin Assignment

No	Symbol	Details	Remark
1	GND	Ground	
2	LED5	Backlight LED Cathode5	
3	LED4	Backlight LED Cathode4	
4	LED3	Backlight LED Cathode3	
5	LED2	Backlight LED Cathode2	
6	LED1	Backlight LED Cathode1	
7	VLED	Power supply for Backlight LED	
8	VLED	Power supply for Backlight LED	
9	NC(TEST)	TEST Pin(PVSS)	Please do not connect anything.
10	GND	Ground	
11	DSI_D1N	MIPI-DSI Data differential signal input pin	
12	DSI_D1P	MIPI-DSI Data differential signal input pin	
13	GND	Ground	
14	DSI_CP	MIPI-DSI Clock differential signal input pin	
15	DSI_CN	MIPI-DSI Clock differential signal input pin	
16	GND	Ground	
17	DSI_D0N	MIPI-DSI Data differential signal input pin	
18	DSI_D0P	MIPI-DSI Data differential signal input pin	
19	GND	Ground	
20	RESETB	LCD Reset	L:Initialize Power_ON Reset is Required when Turning on the Power
21	GND	Ground	
22	VCCIO	DSI and I/O Power Supply	VCCIO = 1.8V(TYP)
23	VDD	Analog Power Supply	VDD = 2.8V(TYP)
24	VDD	Analog Power Supply	VDD = 2.8V(TYP)
25	GND	Ground	

- Recommended connector: HIROSE : FH35C-25S-0.3SHW
- Please make sure to check a consistency between pin assignment in "3.2 Outward Form" and your connector pin assignment when designing your circuit.
  Inconsistency in input signal assignment may cause a malfunction.
- Since FPC cable has gold plated terminals, gilt finish contact shoe connector is recommended.

5. Absolute Maximum Rating

GND=0V

Item	Symbol	Condition	Rating		Unit	Applicable terminal
			MIN	MAX		
Supply voltage	VDD	Ta=25 ℃	-0.3	4.6	V	VDD
DSI and I/O Power Supply voltage	VCCIO		-0.3	4.6	V	VCCIO
Input voltage for logic	VI		-0.3	VCCIO+0.3	V	RESETB
DSI Input voltage	VDSIIN		-0.15	1.45	V	DSI_D0P/N , DSI_D1P/N DSI_CP/N
LED forward current	IL	Ta = 25 ℃	-	30	mA	VLED, LED1～5
		Ta = 70 ℃	-	14		
Storage temperature range	Tstg		-30	80	℃	
Storage humidity range	Hstg	Non condensing in an environmental moisture at or less than 40 ℃ 90%RH.				

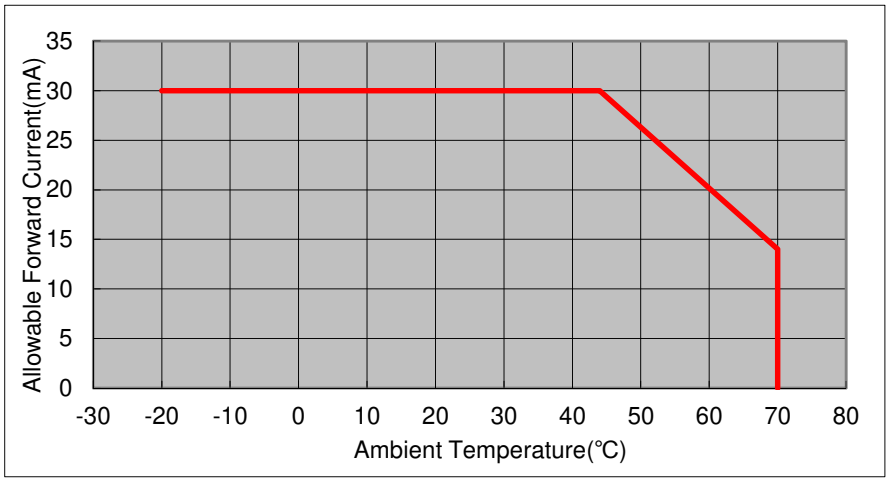
6. Recommended Operating Conditions

GND=0V

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
Supply voltage	VDD		2.7	2.8	2.9	V	VDD
DSI and I/O Power Supply voltage	VCCIO		1.7	1.8	1.9	V	VCCIO
Input voltage for logic	VI		0	-	VCCIO	V	RESETB
DSI Input voltage	VI		-0.05	-	1.35	V	DSI_D0P/N DSI_D1P/N DSI_CP/N
Operational temperature range	Top	Note1,2	-20	25	70	℃	Panel surface temperature
Operating humidity range	Hop	Ta<=40 ℃	20	-	85	%	
		Ta>40 ℃	Non condensing in an environmental moisture at or less than 40 ℃ 85%RH.				

Note1: This monitor is operatable in this temperature range. With regard to optical characteristics, refer to Item 11."CHARACTERISTICS".

Note 2: Acceptable Forward Current to LED is up to 14 mA, when Ta=+70 ℃.
Do not exceed Allowable Forward Current shown on the chart below.



7. Characteristics

7.1 DC Characteristics

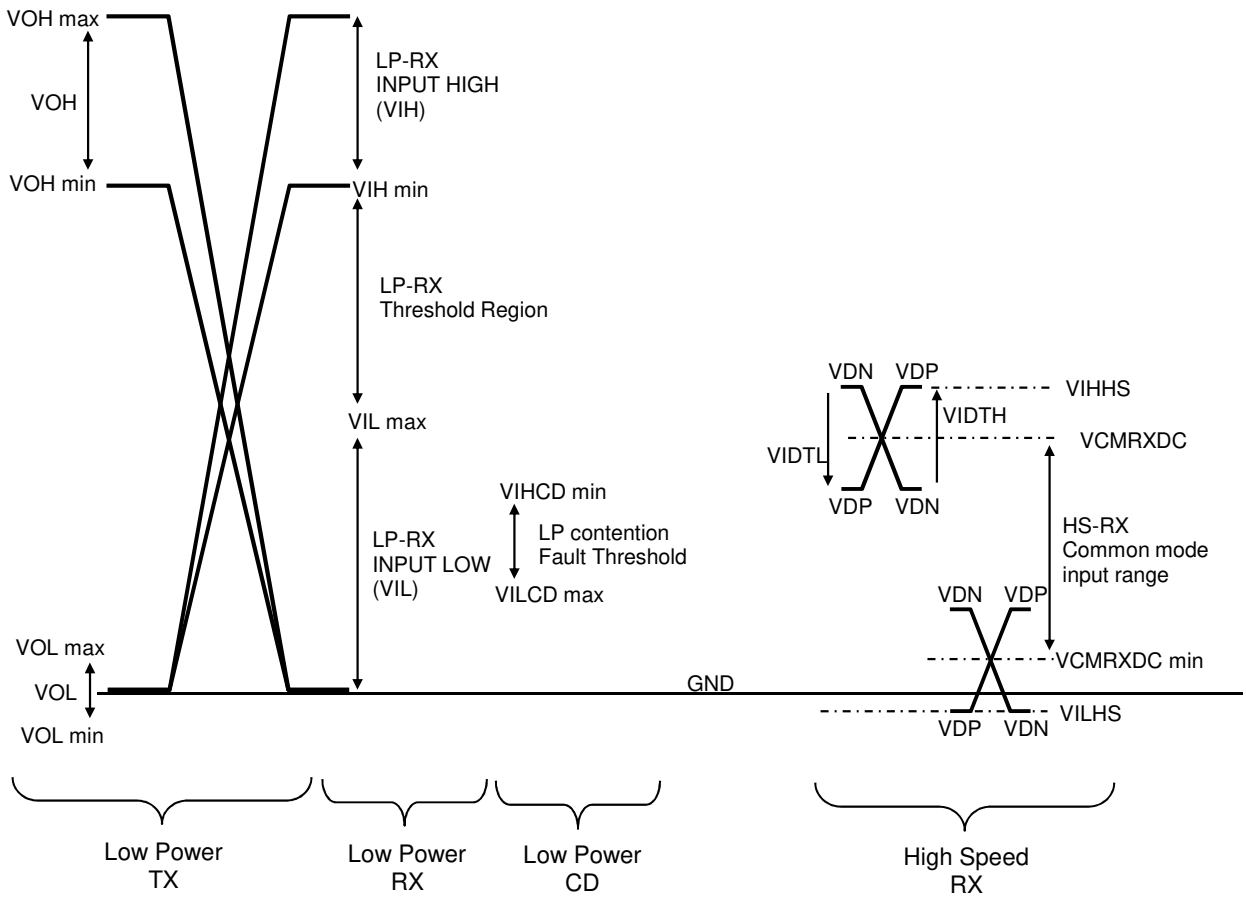
7.1.1 Display Module

(Unless otherwise noted, Ta=25 ℃,VDD=2.8V,VCCIO=1.8V,GND=0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
Input Signal Voltage	VIH	VCCIO=1.7-1.9V	0.7×VCCIO	-	VCCIO	V	RESETB
	VIL		0	-	0.3×VCCIO	V	
Operating Current	IDD	fDSICLK=150 MHz	-	11.2	22.4	mA	VDD
	ICCIO	Color bar display	-	3.5	7.0	mA	VCCIO
Sleep_mode Current	IDDS	Clock/Data=LP11	-	39	100	uA	VDD
	ICCIOS	Sleep_mode	-	17	100	uA	VCCIO

7.1.2 MIPI DSI Interface

Item		Symbol	Condition	Rating			Unit	Note
				MIN	TYP	MAX		
HS-RX	Differential input high threshold	VIDTH		-	-	110	mV	
	Differential input low threshold	VIDTL		-110	-	-	mV	
	Single-ended input high voltage	VIHHS		-	-	460	mV	
	Single-ended input low voltage	VILHS		-40	-	-	mV	
	Common-mode voltage HS receive mode	VCMRXDC		70	-	330	mV	
	Differential input impedance	ZID		80	100	125	Ohm	
LP-RX	Logic 1 input voltage	VIH		880	-	-	mV	
	Logic 0 input voltage	VIL		-	-	550	mV	
LP-TX	Thevenin output low level	VOL		-50	-	50	mV	
	Thevenin output high level	VOH		1.1	1.2	1.3	V	
	Output impedance of LP transmitter	ZOLP		110	-	-	Ohm	
CD-RX	Logic 1 contention threshold	VIHCD		450	-	-	mV	
	Logic 0 contention threshold	VILCD		-	-	220	mV	



The signal levels for the LP and HS .

7.1.3 Backlight

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
Forward current	IL25	Ta=25 ℃	--	8.5	30	mA	VLED,
	IL70	Ta=70 ℃	--	--	14	mA	LED1～5
Forward voltage *	VL	Ta=25 ℃ IL=8.5 mA	2.58	2.80	3.16	V	

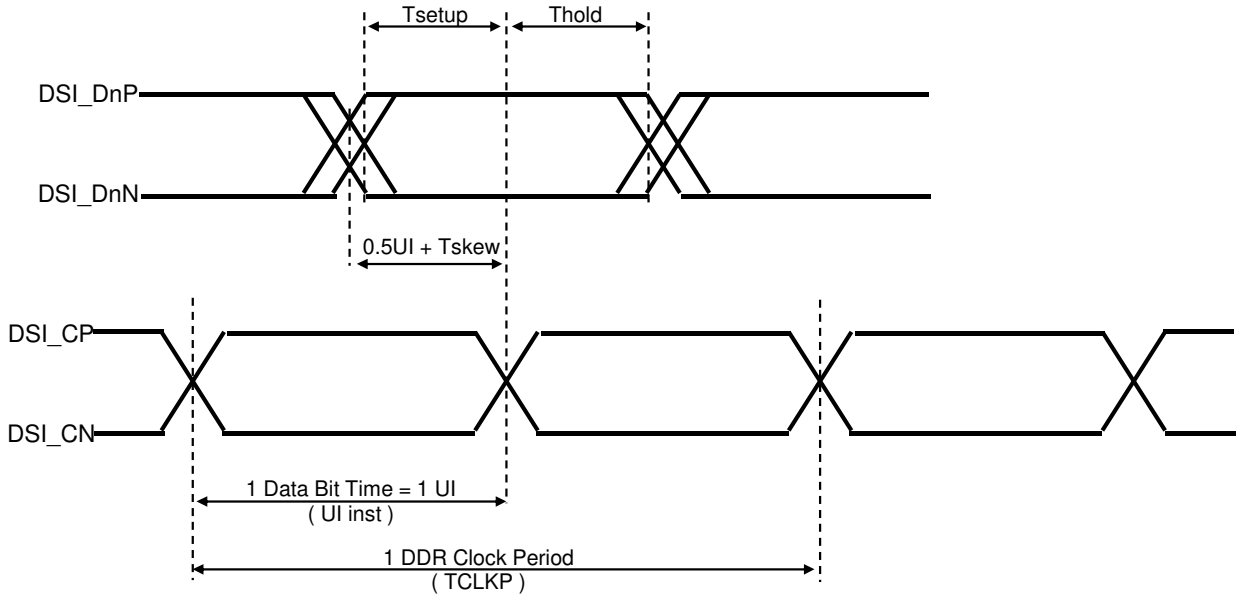
*Reference only

7.2 AC Characteristics

Ⓐ 7.2.1 HS-RX Specifications

(Unless otherwise noted, Ta=25 ℃,VDD=2.8V,VCCIO=1.8V,GND=0V)

Item	Symbol	Rating			Unit	Applicable terminal
		MIN	TYP	MAX		
DSICLK Frequency	f DSICLK	40	-	200	MHz	DSI_CP/N
DSICLK Cycle time	TCLKP	5.0	-	25.0	ns	
DSI Data Transfer Rate	UI	2.5	-	12.5	ns	DSI_D0P/N , DSI_D1P/N
	t DSIR	80	-	400	Mbps	
Data to Clock Setup Time	Tsetup	0.35	-	-	UI	DSI_D0P/N , DSI_D1P/N
Clock to Data Hold Time	Thold	0.25	-	-	UI	DSI_CP/N



Data to Clock Timing Definitions

7.2.2 LP-TX Specifications

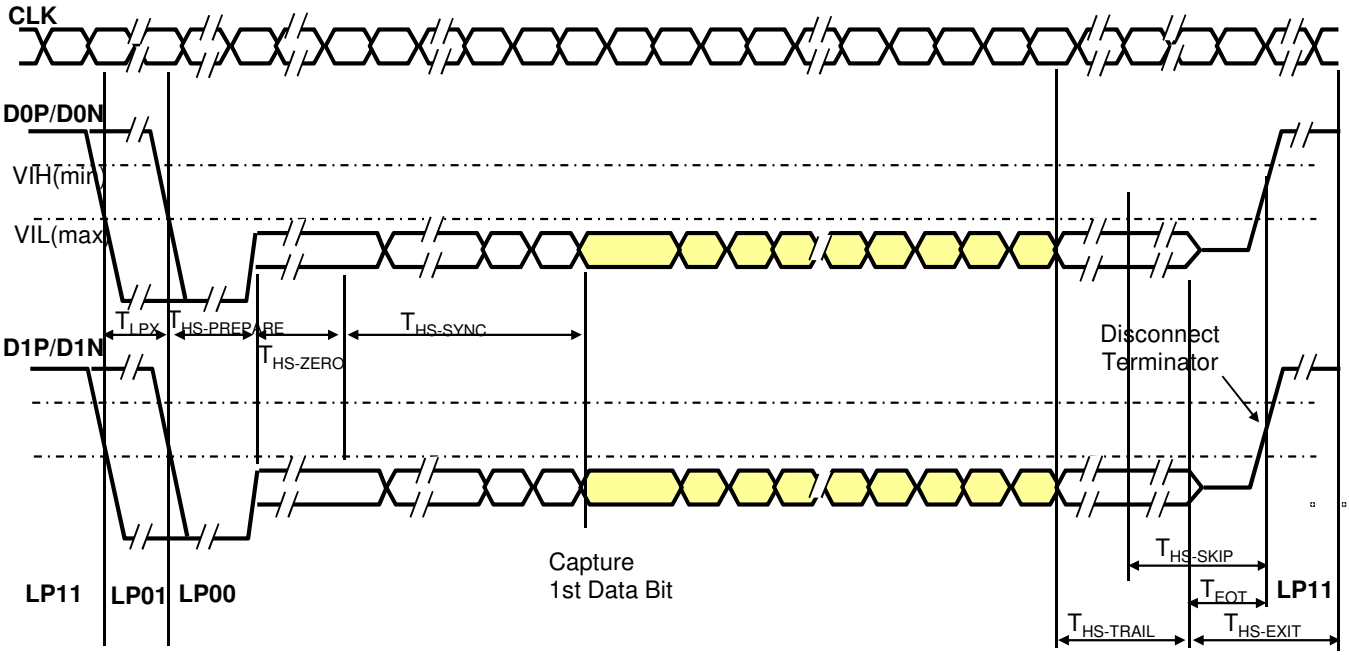
(Unless otherwise noted, Ta=25 ℃,VDD=2.8V,VCCIO=1.8V,GND=0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
15% - 85% rise time	TRLP		-	-	25	ns	DSI_D0P/N
85% - 15% fall time	TFLP		-	-	25	ns	DSI_D0P/N
Slew rate	Δv / ⊿tSR	Cload = 70pF	30	-	500	mV/ns	DSI_D0P/N

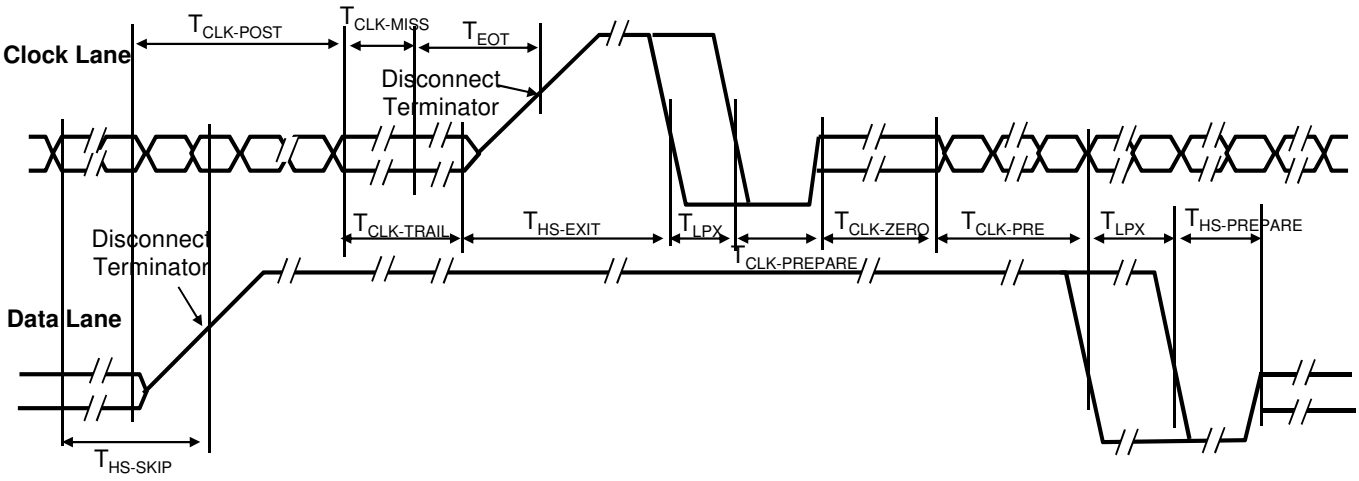
7.2.3 RX/TX Specifications

(Unless otherwise noted, Ta=25 ℃,VDD=2.8V,VCCIO=1.8V,GND=0V)

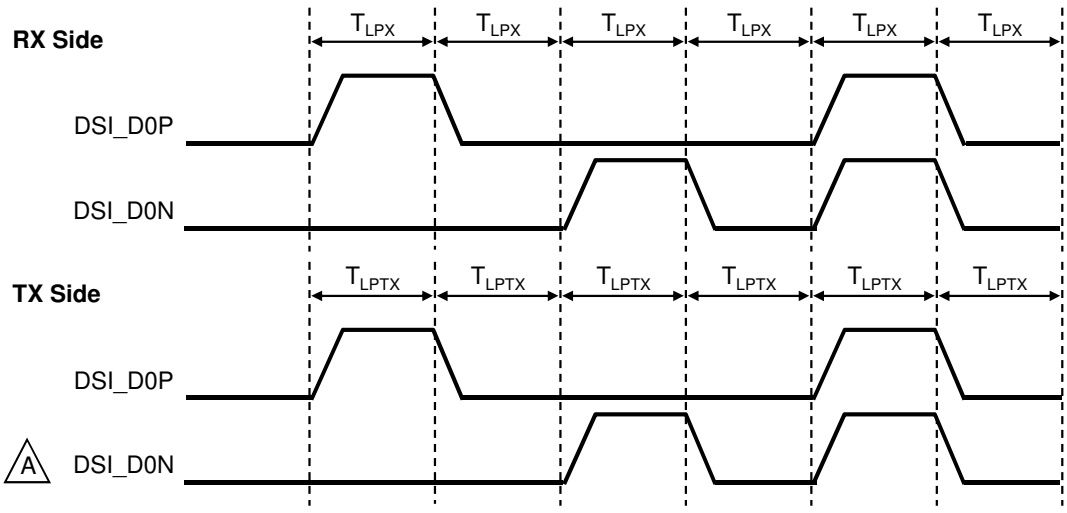
Item	Description	Rating			Unit
		MIN	TYP	MAX	
$T_{HS-PREPARE}$	Time to drive LP00 to prepare for HS transmission	40 ns + 4UI	-	85 ns + 6UI, ≦100 ns	
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS0 before the SYNC sequence	145 ns +10UI	-	-	
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max(n*8UI,60 ns+n*4UI)	-	-	
$T_{HS-EXIT}$	Time to drive LP11 after HS burst	100	-	-	ns
T_{TA-GO}	Time to drive LP00 after Tumaround Request	$4*T_{LPTX}$			
$T_{TA-SURE}$	Time out before new TX side starts driving	TLPTX	-	$2*T_{LPTX}$	
T_{TA-GET}	Time to drive LP00 by new TX	$5*T_{LPTX}$			
T_{LPX}	Length of any Low Power state period	50	-	-	ns
Ratio T_{LPX}	Ratio of T_{LPX}(MASTER)/T_{LPX}(SLAVE) between Master and Slave side	2/3	-	3/2	
$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60 ns + 52UI	-	-	
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ +time for lead HS-0 drive period before starting Clock	300	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
T_{EOT}	Time from start of THS-TRAIL period to start of LP-11 state	-	-	105 ns + n*12UI	
T_{LPTX1}	Length of Low-Power TX state period in case of using DSI clock	-	n*DSITX	-	UI
T_{LPTX2}	Length of Low-Power TX state period in case of using internal OSC clock	-	1/fosc	-	ns



HS Data Transmission in Bursts



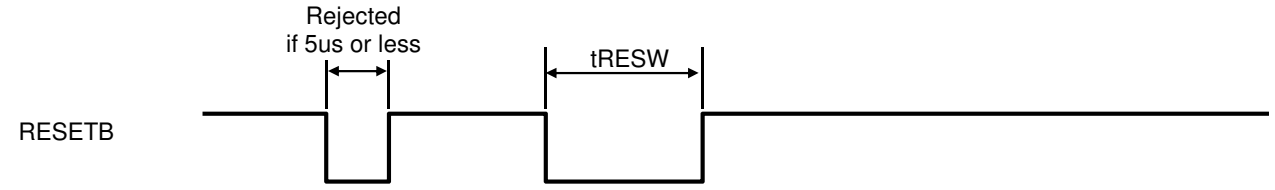
Switching the Clock Lane between Clock Transmission and LP mode



DSI LP Mode

A 7.2.4 Reset input timing

Item	Symbol	Condition	Rating			Unit	Remark
			MIN	TYP	MAX		
Reset Low Pulse width	tRESW		10	-	-	us	



RESETB input timing

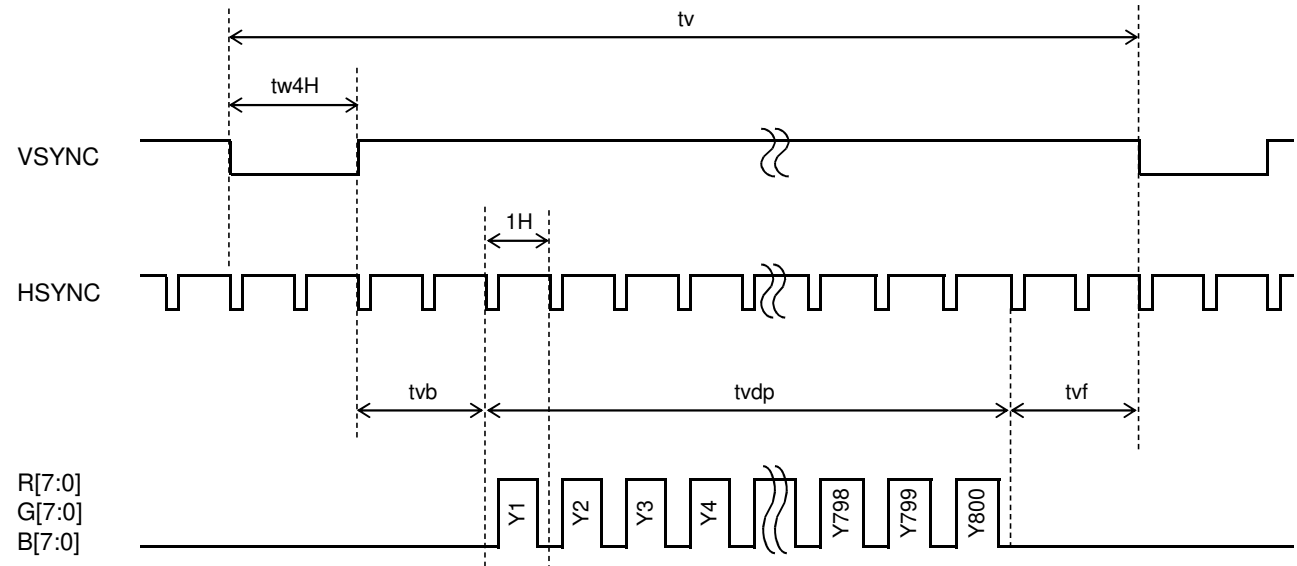
A 7.3 Input Timing Characteristics

Item	Symbol	Rating			Unit	Remark
		MIN	TYP	MAX		
CLK Frequency	fPCLK	--	25.0	--	MHz	PCLK
VSYNC Frequency Note	fVSYNC	54.0	57.5	63.2	Hz	VSYNC
VSYNC Cycle	tv	809	824	850	H	
VSYNC Pulse Width	tw4H	3	8	--	H	
Vertical Back Porch	tvb	3	8	--	H	
Vertical Front Porch	tvf	3	8	--	H	
Vertical Display Period	tvdp	800			H	
HSYNC frequency	fHSYNC	47.3			kHz	HSYNC
HSYNC Cycle	th	504	528	568	CLK	
HSYNC Pulse Width	tw5H	5	16	78	CLK	
Horizontal Back Porch	thb	5	16	78	CLK	
Horizontal Front Porch	thf	5	16	78	CLK	
Horizontal data start Point	tw5H+thb	19	32	83	CLK	
Horizontal Blanking Period	tw5H+thb+thf	24	48	88	CLK	
Horizontal Display Period	thdp	--	480	--	CLK	

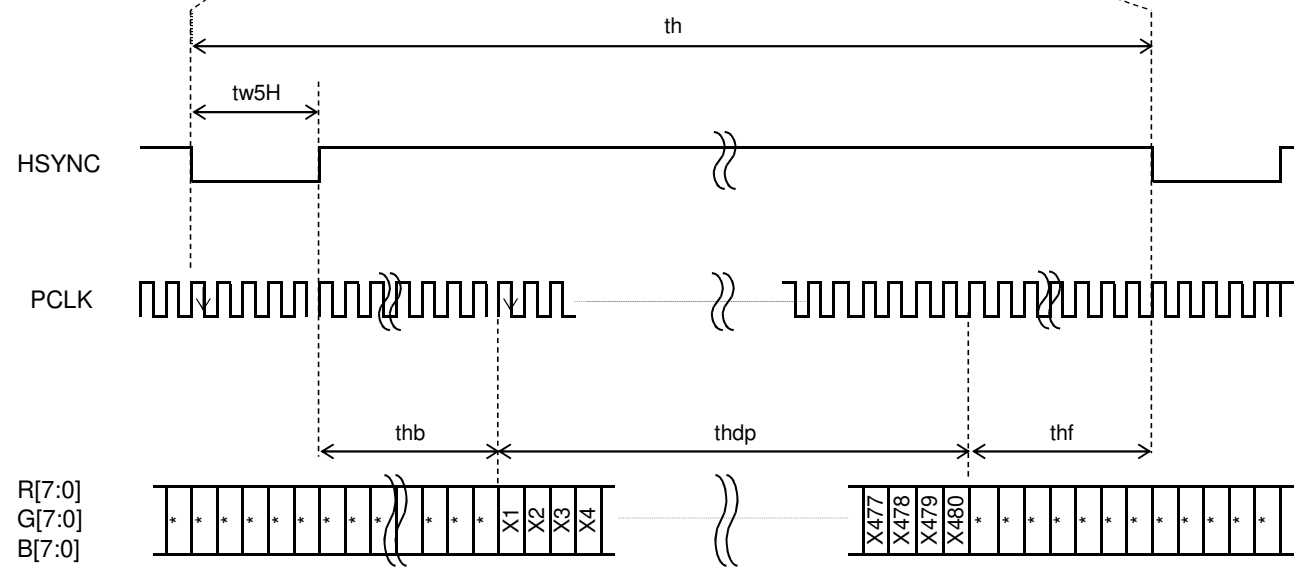
Note: This is recommended spec to get high quality picture on display. It is customer's risk to use out of this frequency.

7.4 Input Signal Timing Chart

-Vertical Timing



-Horizontal Timing



Timing Characteristics of input signals

8. About MIPI Interface

8.1 Version

The DSI incorporated in the LCD-Driver complies with the following standards.

MIPI DSI : Version 1.01

MIPI D-PHY : Version 1.00

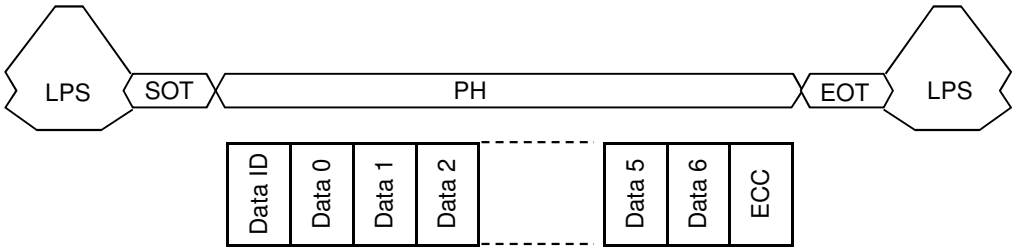
Data transfer mode : Video mode only.

A If the DSI_CLK lane becomes unintentionally at the LP (Low Power) level due to the influence of noise such as ESD, it may malfunction. As a countermeasure for this, we recommend turning DSI_CLK OFF (LP) during the blanking period.

Virtual Channel : Set to VC[1:0]=00.

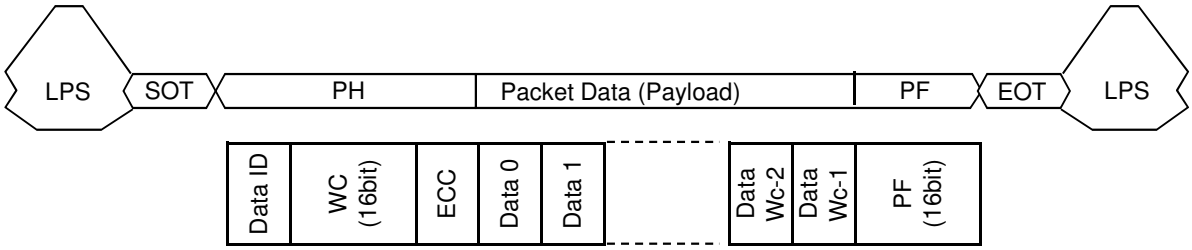
8.2 DSI protocol

- Short packets specify the payload length using the Data Type field and are from 2 to 9 bytes in length. Short packets is used for most Command Mode commands and associated parameters.



LPS : Low power state
SOT : Start of Transmission
PH : Packet Header
DI(Data ID) : Contain Virtual Channel Identifier and Data Type
ECC : Error Correction Code

- Long packets specify the payload length using a two-byte Word Count field and then the payload maybe 0 to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data.



LPS : Low power state
SOT : Start of Transmission
PH : Packet Header
DI(Data ID) : Contain Virtual Channel Identifier and Data Type
WC(Word Count) : The receiver use WC to define packet end.
ECC : Error Correction Code
PF(Packet Footer) : Mean 16-bit Checksum.

8.3 Packet data types

LCD-Driver has the following restriction.

Generic short / Long Write Cmd is not supported.

It is only DCS Short / Long Write Cmd.

Processor to peripheral direction

Data Type Hex	Description	Size
01 h	Sync Event , V Sync Start (01,00,00,07)	Short
11 h	Sync Event , V Sync End (11,00,00,14)	Short
21 h	Sync Event , H Sync Start (21,00,00,12)	Short
31 h	Sync Event , H Sync End (31,00,00,01)	Short
22 h	Shut Down Peripheral Command (22,00,00,1E)	Short
32 h	Turn On Peripheral Command (32,00,00,0D)	Short
05 h	DCS WRITE , no parameters	Short
15 h	DCS WRITE , one parameters	Short
06 h	DCS READ , no parameters	Short
37 h	Set Maximum Return Packet Size	Short
08 h	End of Transmission Packet (08,0F,0F,01)	Short
09 h	Null Packet , no data	Long
19 h	Blanking Packet , no data	Long
39 h	DCS Long Write Command Packet	Long
0E h	Packed Pixel Stream , 16-bit RGB , 5-6-5 Format	Long
1E h	Packed Pixel Stream , 18-bit RGB , 6-6-6 Format	Long
2E h	Loosely Packed Pixel Stream , 18-bit RGB ,6-6-6 Format	Long
3E h	Packed Pixel Stream , 24-bit RGB , 8-8-8 Format	Long

Peripheral to processor direction

Data Type Hex	Description	Size
02 h	Acknowledge with Error Report	Short
1C h	DCS Long READ Response	Long

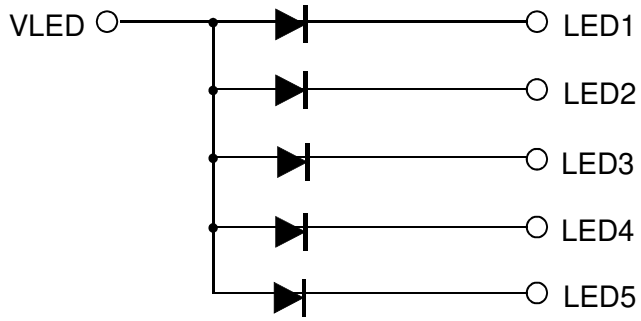
8.4 Packet Footer on the long packet

After Packet Data, Packet Footer is added in Long packet. Packet Footer adds CRC calculated from Packet Data as Checksum.

Checksum(2byte) = CRC(Packet Data)

CRC = X^16 + X^12 + X^5 + X^0

10. LED Circuit



11. Characteristics

11.1 Optical Characteristics

< Measurement Condition >

Measuring instruments: CS2000（KONICA MINOLTA）, LCD7200(OTSUKA ELECTRONICS）, EZcontrast160D（ELDIM）

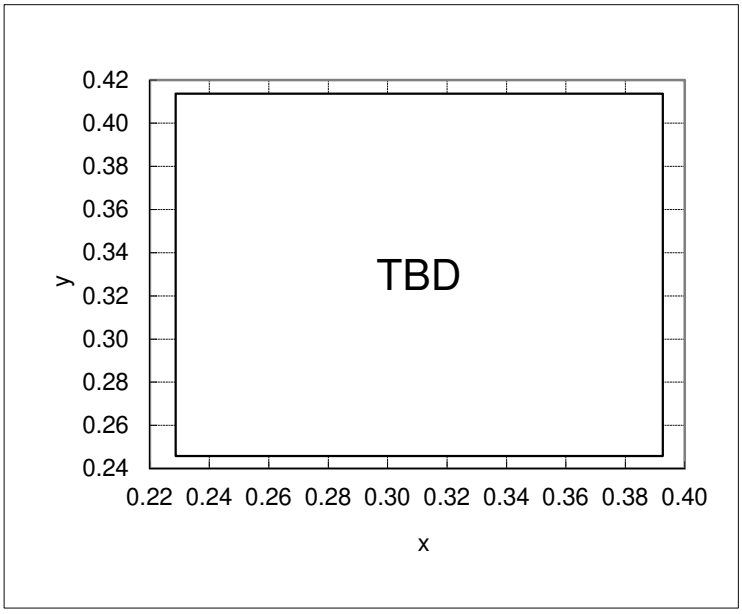
Driving condition: VDD=2.8V,VCCIO=1.8V
Optimized VCOMDC

Backlight: IL=(8.5)mA

Measured temperature: Ta=25°C

Item		Symbol	Condition	MIN	TYP	MAX	Unit	Note No.	Remark
Response time	Rise time	TON	[Data]= 00h→FFh	—	—	(40)	ms	1	※
	Fall time	TOFF	[Data]= FFh→00h	—	—	(60)	ms		
Contrast ratio	Backlight ON	CR	[Data]= FFh / 00h	(400)	(800)	—		2	
	Backlight OFF			—	(2.9)	—			
Viewing angle	Left	θL	[Data]= FFh / 00h CR≧10	(80)	—	—	deg	3	※
	Right	θR		(80)	—	—	deg		
	Up	φU		(80)	—	—	deg		
	Down	φD		(80)	—	—	deg		
White Chromaticity		x		White chromaticity range				4	
		y							
Burn-in				No noticeable burn-in image shall be observed after 2 hours of window pattern display.				5	
Center brightness			[Data]=FFh	(240)	(380)	—	cd/m^2	6	
Brightness distribution			[Data]=FFh	(70)	—	—	%	7	

* Note number 1 to 7: Refer to the APPENDIX of "Reference Method for Measuring Optical Characteristics".



White Chromaticity Range

【White Chromaticity Range】

x	y
TBD	TBD
TBD	TBD
TBD	TBD
TBD	TBD
TBD	TBD
TBD	TBD

11.2 Temperature Characteristics

< Measurement Condition >
Measuring instruments: CS2000（KONICA MINOLTA）, LCD7200(OTSUKA ELECTRONICS）
Driving condition: VDD=2.8V,VCCIO=1.8V
Optimized VCOMDC
Backlight: IL=(8.5)mA

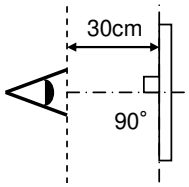
Item			Specification		Remark
			Ta＝-20°C	Ta＝70˚C	
Contrast ratio		CR	(200) or more	(200) or more	Backlight ON
Response time	Rise time	TON	(400) msec or less	(30) msec or less	
	Fall time	TOFF	(600) msec or less	(50) msec or less	
Display Quality			No noticeable display defect or ununiformity should be observed.		

12. Criteria of Judgment

12.1 Defective Display and Screen Quality

Test Condition: Observed TFT-LCD monitor from front during operation with the following conditions

Driving Signal	Raster Pattern (RGB, white, black)
Signal condition	[Data]: 00h, (BC)h, FFh (3steps)
Observation distance	30 cm
Illuminance	200 to 350 lx
Backlight	IL=(8.5)mA



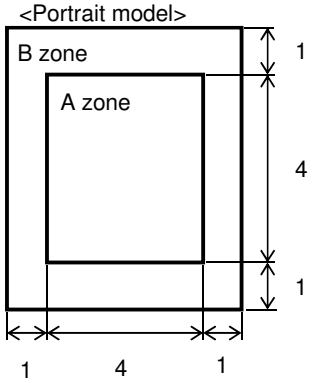
Defect item		Defect content		Criteria
Display Quality	Line defect	Black, white or color line, 3 or more neighboring defective dots		Not exists
	Dot defect	Uneven brightness on dot-by-dot base due to defective TFT or CF, or dust is counted as dot defect (brighter dot, darker dot) High bright dot: Visible through 2% ND filter at [Data]=00h Low bright dot: Visible through 5% ND filter at [Data]=00h Dark dot: Appear dark through white display at [Data]=(BC)h		Refer to table 1
		Invisible through 5% ND filter at [Data]=00h		Acceptable
Screen Quality	Dirt	Uneven brightness (white stain, black stain etc)		Invisible through 5% ND filter at Black screen. Invisible through 1% ND filter at other screen.
	Foreign particle	Point-like	0.25mm< φ	N=0
			0.20mm< φ ≦0.25mm	N≦2
			φ ≦0.20mm	Acceptable
		Liner	3.0mm<length and 0.08mm<width	N=0
			length≦3.0mm or width≦0.08mm	Acceptable
	Others			Use boundary sample for judgment when necessary

φ(mm): Average diameter = (major axis + minor axis)/2
Permissible number: N

Table 1

Area	High bright dot	Low bright dot	Dark dot	Total	Criteria
A	0	2	2	3	Permissible distance between same color bright dots (includes neighboring dots): 3 mm or more Permissible distance between same color high bright dots (includes neighboring dots): 5 mm or more
B	2	4	4	6	
Total	2	4	4	6	

<Portrait model>



Division of A and B areas
B area: Active area
Dimensional ratio between A and B areas: 1: 4: 1
(Refer to the left figure)

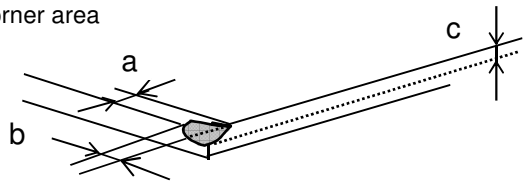
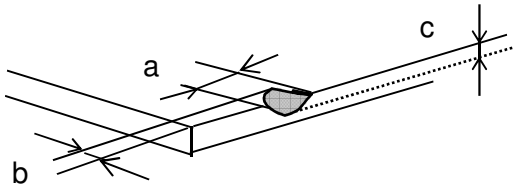
12.2 Screen and Other Appearance

Testing conditions

Observation distance 30cm

Illuminance 1200～2000 lx

Item		Criteria	Remark
Polarizer	Flaw Stain Bubble Dust Dent	Ignore invisible defect when the backlight is on.	Applicable area: Active area only (Refer to the section 3.2 "Outward form")
S-case		No functional defect occurs	
FPC cable		No functional defect occurs	

Item	Appearance	Criteria
Glass chipping	Corner area  	Unit:mm a≦3 b≦3 c≦t (t: glass thickness) a,b≦0.5 is acceptable n≦2
	Others  	Unit:mm a≦5 b≦1 c≦t (t:glass thickness) a,b≦0.5 is acceptable Maximum permissible number of chipping off on a side is 5.
	Progressive crack	None

13. Reliability Test

Test item		Test condition	number of failures /number of examinations
Durability test	High temperature storage	Ta=80°C 240hrs	TBD
	Low temperature storage	Ta=-30°C 240hrs	TBD
	High temperature & high humidity storage	Ta=60°C, RH=90% 240hrs non condensing ※	TBD
	High temperature operation	Tp=70°C 240hrs	TBD
	Low temperature operation	Tp=-20°C 240hrs	TBD
	High temp & humid operation	Tp=40°C, RH=90% 240hrs non condensing ※	TBD
	Thermal shock storage	-30←→80°C(30min/30min) 100 cycles	TBD
	Lightfastness	Xenon Blackpanel 63±3℃ non-shower 450W/m^2（300～700nm） non-operating Integral dose 800MJ/m^2	TBD
Mechanical environmental test	Electrostatic discharge test (Non operation)	Confirms to EIAJ ED-4701/300 C=200pF,R=0Ω,V=±200V Each 3 times of discharge on and power supply and other terminals.	TBD
	Surface discharge test (Non operation)	C=250pF, R=100Ω, V=±TBDkV Each 5 times of discharge in both polarities on the center of screen with the case grounded.	TBD
	Vibration test	Total amplitude 1.5mm, f=10～55Hz, X,Y,Z directions for each 2 hours	TBD
	Impact test	Use TOPPAN PRINTING original jig (see next page)and make an impact with peak acceleration of 1000m/s2 for 6 msec with half sine-curve at 3 times to each X, Y, Z directions in conformance with JIS C 60068-2-27-2011.	TBD
Packing test	Packing vibration-proof test	Acceleration of 19.6m/s^2 with frequency of 10→55→10Hz, X,Y, Zdirection for each 30 minutes	TBD
	Packing drop test	Drop from 75cm high. 1 time to each 6 surfaces, 3 edges, 1 corner	TBD

Note:Ta=ambient temperature Tp=Panel temperature

※ The profile of high temperature/humidity storage and High Temperature/humidity operation
(Pure water of over 10MΩ·cm shall be used.)

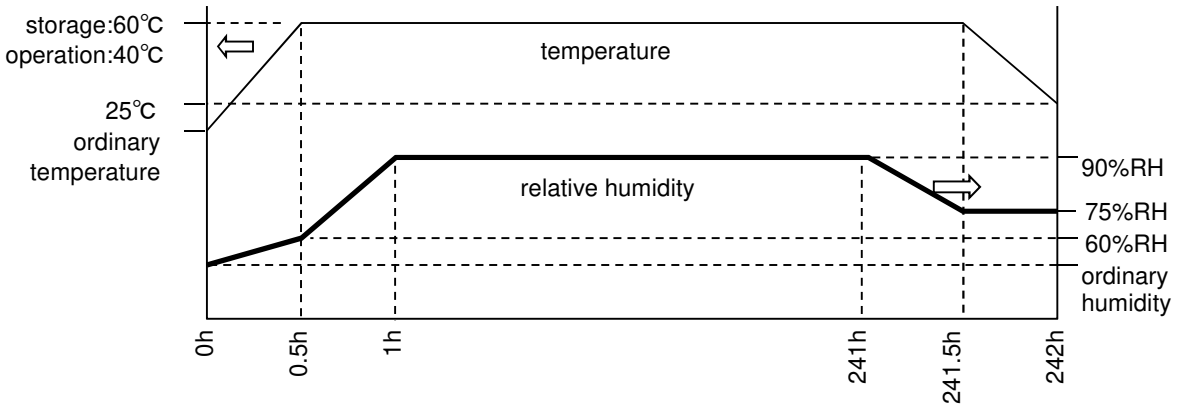
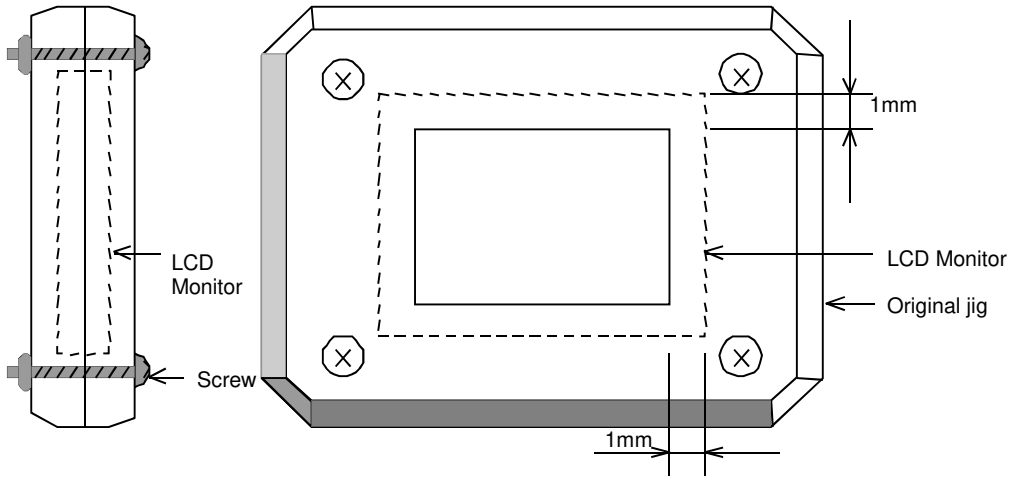


Table2.Reliability Criteria

The parameters should be measured after leaving the monitor at the ordinary temperature for 24 hours or more after the test completion.

item	Standard	Remarks
Display quality	No visible abnormality shall be seen. (Except for unevenness by Pol deterioration.)	
Contrast ratio	200 or more	Backlight ON

TOPPAN PRINTING Original Jig



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